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## UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

### APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1.  Fee Transmittal Form (e.g., PTO/SB/17)  
(Submit an original and a duplicate for fee processing)
2.  Applicant claims small entity status.  
See 37 CFR 1.27.
3.  Specification [Total Pages 25]  
(preferred arrangement set forth below)
  - Descriptive title of the invention
  - Cross Reference to Related Applications
  - Statement Regarding Fed sponsored R & D
  - Reference to sequence listing, a table, or a computer program listing appendix
  - Background of the Invention
  - Brief Summary of the Invention
  - Brief Description of the Drawings (if filed)
  - Detailed Description
  - Claim(s)
  - Abstract of the Disclosure
4.  Drawing(s) (35 U.S.C. 113) [ Total Sheets 14 ]
5. Oath or Declaration [ Total Pages 3 ]
  - a.  Newly executed (original or copy)
  - b.  Copy from a prior application (37 CFR 1.63 (d))  
(for continuation/divisional with Box 17 completed)
    - i.  **DELETION OF INVENTOR(S)**  
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6.  Application Data Sheet. See 37 CFR 1.76

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:

Continuation    Divisional    Continuation-in-part (CIP)

of prior application No.: \_\_\_\_\_ / \_\_\_\_\_

Prior application information: Examiner \_\_\_\_\_

Group / Art Unit: \_\_\_\_\_

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

### 18. CORRESPONDENCE ADDRESS

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# FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT (\$ 521.00)

## Complete if Known

Application Number	
Filing Date	OCT 2000
First Named Inventor	Kenneth J. Kledzik
Examiner Name	
Group Art Unit	
Attorney Docket No.	LE99-02

## METHOD OF PAYMENT

1.  The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

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Under 37 CFR 1.16 and 1.17

Applicant claims small entity status.  
See 37 CFR 1.27

2.  Payment Enclosed:

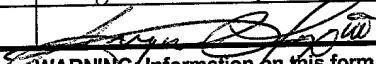
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## FEE CALCULATION (continued)

## 3. ADDITIONAL FEES

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
105	130	205 65 Surcharge - late filing fee or oath	
127	50	227 25 Surcharge - late provisional filing fee or cover sheet	
139	130	139 130 Non-English specification	
147	2,520	147 2,520 For filing a request for ex parte reexamination	
112	920*	112 920* Requesting publication of SIR prior to Examiner action	
113	1,840*	113 1,840* Requesting publication of SIR after Examiner action	
115	110	215 55 Extension for reply within first month	
116	390	216 195 Extension for reply within second month	
117	890	217 445 Extension for reply within third month	
118	1,390	218 695 Extension for reply within fourth month	
128	1,890	228 945 Extension for reply within fifth month	
119	310	219 155 Notice of Appeal	
120	310	220 155 Filing a brief in support of an appeal	
121	270	221 135 Request for oral hearing	
138	1,510	138 1,510 Petition to institute a public use proceeding	
140	110	240 55 Petition to revive - unavoidable	
141	1,240	241 620 Petition to revive - unintentional	
142	1,240	242 620 Utility issue fee (or reissue)	
143	440	243 220 Design issue fee	
144	600	244 300 Plant issue fee	
122	130	122 130 Petitions to the Commissioner	
123	50	123 50 Petitions related to provisional applications	
126	240	126 240 Submission of Information Disclosure Stmt	
581	40	581 40 Recording each patent assignment per property (times number of properties)	40
146	710	246 355 Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249 355 For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279 355 Request for Continued Examination (RCE)	
169	900	169 900 Request for expedited examination of a design application	
Other fee (specify) _____			
Reduced by Basic Filing Fee Paid			SUBTOTAL (3) (\$ 40)

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SUBMITTED BY		Complete (if applicable)		
Name (Print/Type)	Angus C. Fox, III	Registration No. (Attorney/Agent)	31,828	Telephone 801-225-9000
Signature		Date	10 OCT 2000	

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## CARRIER-BASED ELECTRONIC MODULE

5 This invention is related to two U.S. patent applications, the first of which is application serial number 09/285,354, which was filed on April 2, 1999, and which is titled ELECTRONIC MODULE HAVING A THREE DIMENSIONAL ARRAY OF INTEGRATED CIRCUIT PACKAGES, the second of which is application serial number 09/524,324, which was filed on March 13, 2000, and which is titled ELECTRONIC MODULE HAVING A THREE DIMENSIONAL ARRAY OF INTEGRATED CIRCUIT PACKAGES.

### FIELD OF THE INVENTION

10 This invention relates to the production of multi-chip electronic modules, and more particularly to a method and apparatus for attaching multiple integrated circuit packages to printed circuit boards. It also relates to high-density memory modules having three-dimensional arrangements of integrated circuit packages.

### BACKGROUND OF THE INVENTION

15 Demand for semiconductor memory is highly elastic. When such memory is relatively inexpensive compared to the overall cost of a computer system, an almost unsatisfiable demand results, with computer manufacturers tending to install an amount of main memory in each system that greatly exceeds the amount required for average program use. On the other hand, when it is costly, manufacturers typically install an amount in each system that only marginally fulfills the requirement of the average program. Although the sales prices of computers may, thus, be maintained at low 20 levels, the end user may soon find that he must upgrade his computer's main memory.

25 The ever increasing demand for large random access computer memories, and the growing demand for increasingly compact computers, coupled with an incentive on the part of the semiconductor manufactureres to reduce the cost per bit, has lead to not only a quadrupling of circuit density approximately every three years, but to increasingly efficient techniques for packaging and mounting the circuit chips. Up until the late 1980's, semiconductor memory chips were usually packaged as dual in-line pin packages (DIPPs). The pins of these DIPP packages were generally soldered directly 30 within through-holes in a circuit board (e.g., the motherboard), or they were inserted in sockets which were, in turn, soldered within through-holes in the circuit board. With the

advent of surface mount technology, conventional plated through-holes on printed circuit boards have been replaced with conductive mounting pads. Small Outline J-lead (SOJ) packages have led to Thin Small Outline Packages (TSOPs). Because the pitch or spacing between centers of adjacent surface mount pins is significantly less than the conventional 0.10-inch spacing for conventional through-hole components, surface mount chips tend to be considerably smaller than corresponding conventional chips, thus taking up less space on a printed circuit board. Additionally, as through holes are no longer needed, surface mount technology lends itself to the mounting of components on both sides of a printed circuit board. Memory modules utilizing surface-mount packages on both sides have become the standard. Both the earlier single in-line memory modules (SIMMs) and the currently used dual in-line memory modules (DIMMs) are inserted into sockets on the motherboard.

Packaging density may be increased rather dramatically by fabricating modules in which a plurality of integrated circuit (IC) chips, such as memory chips, are stacked in a three dimensional arrangement. As a general rule, the three-dimensional stacking of chips requires complex, non-standard packaging methods.

One example of a vertical stack of IC chips is provided by U.S. Pat. No. 4,956,694 to Floyd Eide, titled INTEGRATED CIRCUIT CHIP STACKING. A plurality of integrated circuits are packaged within chip carriers and stacked, one on top of the other, on a printed circuit board. Except for the chip select terminal, all other like terminals on the chips are connected in parallel.

Another example of chip stacking is given in U.S. Pat. No. 5,128,831 to Fox, et al. titled HIGH-DENSITY ELECTRONIC PACKAGE COMPRISING STACKED SUB-MODULES WHICH ARE ELECTRICALLY INTERCONNECTED BY SOLDER-FILLED VIAS. The package is assembled from individually testable sub-modules, each of which has a single chip bonded thereto. The sub-modules are interleaved with frame-like spacers. Both the sub-modules and the spacers have alignable vias which provide interconnection between the various sub-modules.

U.S. Pat. No. 5,313,096, also issued to Floyd Eide and titled IC CHIP PACKAGE HAVING CHIP ATTACHED TO AND WIRE BONDED WITHIN AN OVERLYING SUBSTRATE, is another example. Such a package includes a chip having an upper

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active surface bonded to the lower surface of a lower substrate layer having conductive traces on its upper surface which terminate in conductive pads on its periphery.

Connection between terminals on the active surface and the traces is made with wire bonds through apertures within the lower substrate layer. An upper substrate layer, which is bonded to the lower substrate layer, has apertures which coincide with those of the lower substrate layer and provide space in which the wire bonding may occur. After wire bonding has occurred, the apertures are filled with epoxy to form an individually testable sub-module. Multiple sub-modules can be stacked and interconnected with metal strips attached to their edges.

10 A final example of a stacked-chip module is disclosed in U.S. Pat. No. 5,869,353 to A. U. Levy, et al. titled MODULAR PANEL STACKING PROCESS. A plurality of panels are fabricated having apertures therein, an array of chip-mounting pads at the bottom of the apertures, and interfacing conductive pads. Both the chip-mounting pads and the interfacing conductive pads are coated with solder paste. Plastic-encapsulated surface-mount IC chips are positioned on the paste-covered mounting pads, multiple panels are stacked in a layered arrangement and the stack is heated to solder the chip leads to the mounting pads and the interfacing pads of adjacent panels together. Individual chip package stacks are then separated from the panel stack by a cutting and cleaving operation.

20 As can be seen by the foregoing examples, increased chip density is achieved through the use of complicated packaging and stacking arrangements, which must necessarily be reflected in a higher costs per bit of storage.

#### SUMMARY OF THE INVENTION

25 The present invention provides for an improved multi-chip module having increased chip density. All embodiments of the improved module include a circuit board having an array of electrical interconnection pads to which are mounted a plurality of IC package units. Each IC package unit includes multiple IC packages, which are mounted on both opposing sides of a package carrier. The package units may be mounted on one or both sides of the circuit board.

A first embodiment of the invention employs a laminar package carrier having a pair of major planar surfaces. Each planar surface incorporates electrical contact pads. At least one IC package is surface mounted on each major planar surface, by interconnecting the connection elements of the package with the contact pads on the planar surface, to form the IC package unit. Each unit is mounted within its own recess in the circuit board, with one IC package being right-side up, and the other being upside-down. The upside-down IC package may be in contact with a heat sink layer embedded within the circuit board. If corresponding contact pads on both sides of the package carrier are interconnected within the carrier body, contact may be made between the connection elements, or leads, of the IC package closest to the circuit board and the interconnection pads thereon. Using this interconnection technique, the chip carrier may be either a rigid or semi-rigid laminar substrate or it may be a thin film carrier. For another variation of this first embodiment, the laminar substrate package carrier may be modified to incorporate its own set of interconnection leads which mate with the interconnection pads on the circuit board. Greater flexibility is provided by this technique, as rerouting of lead positions may take place within the carrier body. In addition, if connection elements on one IC package must be connected independently with respect to corresponding connection elements on the other package of the package pair (e.g., chip select leads), additional carrier leads may be provided to accomplish the independent connections.

A second embodiment of the invention utilizes a carrier substrate which has at least one recess on each opposing surface for back-to-back surface mounting of the IC packages. IC packages mounted on opposite sides of the carrier may be in contact with opposite sides of a heat sink layer embedded within the carrier substrate. Each resulting IC package unit is surface mounted to the circuit board. If the leads of both packages are interconnected on the carrier, then connection to the circuit board may be made by attaching the leads of only one package directly to the circuit board. However, like the first embodiment, the package carrier may be equipped with its own leads which are connected to the various leads of the mounted IC packages. In such a case, the package carrier leads are directly connected to the interconnection pads on the circuit board.

Third and fourth embodiments of the invention utilize a third embodiment IC package unit having carriers which incorporate features of both the first and second embodiments. One of the packages is mounted on a planar surface of the carrier right-side up, while the other package is mounted on the carrier in a recess upside down.

5 Two different embodiments of modules result because the carrier may be mounted on two types of circuit boards. Either the IC package that is mounted on the planar surface of the carrier, or the IC package that is mounted within the recess, may be mounted adjacent to the circuit board. In the former case, the adjacent package of the package unit fits within a recess on the circuit board. In the latter case, the adjacent package of the package unit mounts on a planar surface of the circuit board. As in the other 10 embodiments, the carrier may be equipped with its own set of interconnection leads which interface with the interconnection pads on the circuit board. Likewise, if the leads of one package are interconnected with those of the other package on the carrier, connection to the circuit board may be made with the leads of the adjacent package.

A fifth embodiment module utilizes a fourth embodiment IC package unit. The primary difference between the fourth embodiment carrier and third embodiment carrier is the addition of carrier leads to the former, the leads being used to attach the fourth embodiment package unit to a circuit board.

20 A sixth embodiment module utilizes a fifth embodiment IC package unit having a flexible thin film substrate. In most other respects, this IC package unit is similar to the first embodiment IC package unit.

25 A seventh embodiment module utilizes a sixth embodiment IC package unit having ball-grid-array type IC packages. Because the connection elements (the pads and attached balls) are oriented face down against the surface of the carrier, this particular package unit utilizes carrier leads to make connection to the printed circuit board.

30 For any of the seven module embodiments, electrical connection between electrical traces on the carrier and electrical traces on the circuit board may be accomplished using one of several commonly used interconnection techniques, such as solder reflow, solder dot bridges, or ball grid joints. In the case where the carrier itself is equipped with leads, leads of the "J" or gull-wing type may be used, with the latter type

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being the preferred.

The invention may be utilized to increase memory density on memory modules. For other types of IC packages, it may be employed to more efficiently utilize available real estate on a printed circuit board.

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#### DESCRIPTION OF THE DRAWINGS

Figure 1 is an exploded isometric view of a first embodiment of an IC package unit, which has a laminar substrate carrier with two major planar surfaces, each major planar surface having an array of mounting pads to which a single IC package may be mounted;

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Figure 2 is an isometric view of the assembled package unit of Figure 1;

Figure 3 is an isometric view of an exploded first embodiment electronic module incorporating multiple first embodiment IC package units;

Figure 4 is an isometric view of the assembled first embodiment electronic module of Figure 3;

Figure 5 is a cross-sectional view of the assembled first embodiment electronic module of Figure 4;

Figure 6 is an exploded isometric view of a second embodiment of an IC package unit, which has an IC chip carrier with a pair of recesses for back-to-back surface mounting of the IC package pair;

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Figure 7 is an isometric view of the assembled package unit of Figure 6;

Figure 8 is an isometric view of an exploded second embodiment electronic module incorporating multiple second embodiment IC package units;

Figure 9 is an isometric view of the assembled second embodiment electronic module of Figure 8;

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Figure 10 is a cross-sectional view of the second embodiment assembled electronic module of Figure 9;

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Figure 11 is an exploded isometric view, from above, of a third embodiment of an IC package unit, which has an IC chip carrier with one major planar surface for mounting one IC chip and a recess on the opposite side thereof for stacked mounting of the IC package pair;

Figure 12 is an isometric view, from above, of the assembled package unit of Figure 11;

Figure 13 is an exploded isometric view, from below, of the third embodiment of the IC package unit shown in Figure 11;

5 Figure 14 is an isometric view, from below, of the assembled package unit of Figure 12;

Figure 15 is an isometric view of an exploded third embodiment electronic module incorporating multiple third embodiment IC package in combination with a circuit board having a pair of opposing major planar surfaces;

10 Figure 16 is an isometric view of the assembled third embodiment electronic module of Figure 15;

Figure 17 is an isometric view of an exploded fourth embodiment electronic module incorporating multiple third embodiment IC package units in combination with a circuit board having a pair of opposing faces, each of which is equipped with multiple chip-receiving recesses;

Figure 18 is an isometric view of the assembled fourth embodiment electronic module of Figure 17;

Figure 19 is a cross-sectional view of the assembled third embodiment assembled electronic module of Figure 16;

20 Figure 20 is a cross-sectional view of the fourth embodiment assembled electronic module of Figure 18;

Figure 21 is an exploded isometric view, from above, of a fourth embodiment IC package unit, which includes a laminar IC chip carrier having its own sets of leads;

25 Figure 22 is an isometric view, from above, of the assembled package unit of Figure 21;

Figure 23 is an exploded isometric view, from below, of the exploded IC package unit of Figure 21;

Figure 24 is an isometric view, from below, of the assembled package unit of Figure 22;

30 Figure 25 is an exploded isometric view of a fifth embodiment electronic module incorporating multiple fourth embodiment IC package units;

Figure 26 is an isometric view of the assembled fifth embodiment electronic module of Figure 25;

Figure 27 is an exploded view of a fifth embodiment IC package unit, which is a variant of the first embodiment IC package unit, in which the laminar carrier is replaced with a flexible thin film carrier;

Figure 28 is a cross-sectional view of an assembled fifth embodiment IC package unit;

Figure 29 is an exploded isometric view of a sixth embodiment IC package unit incorporating four ball-grid-array IC packages;

Figure 30 is an isometric view of the assembled sixth embodiment IC package unit of Figure 29;

Figure 31 is an isometric view of the assembled sixth embodiment IC package unit of Figure 29 mounted on a portion of a printed circuit board;

Figure 32 is an isometric view of a seventh embodiment module having 8 IC package units;

Figure 33 is an isometric view of a variant of the sixth embodiment IC package unit having but two IC packages thereon; and

Figure 34 is an isometric view of the assembled IC package unit of Figure 33 mounted on a portion of a printed circuit board.

#### DETAILED DESCRIPTION OF THE INVENTION

The present invention provides for an improved multi-chip module having increased chip density over conventional modules presently in use. All embodiments of the improved module include a circuit board having an array of electrical interconnection pads to which are mounted a plurality of IC package units. Each IC package unit includes a package carrier having multiple IC packages, which are mounted on opposite sides of the package carrier. The package units may be mounted on one or both sides of the circuit board. The connection elements (leads or pads) of each of the packages are coupled to a carrier interface, which may or may not include

discrete carrier leads.

A first embodiment of the invention, shown in Figures 1 through 5, utilizes a laminar package carrier 101 having a pair of major planar surfaces 102A and 102B. Each major planar surface incorporates at least one set of carrier contact pads 103, each set being configured to receive, by surface mounting, the connection elements, or leads, 104 of an integrated circuit (IC) package 105 of the TSOP (Thin Small Outline Package) type. In this particular example, the leads 104 of an IC package 105 are attached to each contact pad set 103. The resulting assembly, shown in Figure 2, constitutes a first embodiment IC package unit 201.

Referring now to Figure 3, multiple first embodiment package units 201 (in this example, four) are shown ready for mounting on a circuit board 301. In this example, two package units 201A and 201B will be mounted on the upper surface 302U of the circuit board 301, while two package units 201C and 201D will be mounted on the lower surface 302L thereof. One IC package 105H of each package unit 201 fits within its own recess 303 in the circuit board 301 so that it is completely hidden from view, while the other IC package 105E is completely exposed. The surrounding edges of each recess are equipped with a set of board electrical connection contact pads 304. The leads of each hidden package 105H will make direct contact with the contact pads of its recess and will be routed within the circuit board 301 to the appropriate interconnection sites. The leads 104 of the exposed IC package 105E are coupled to the leads 104 of the connections which penetrate the laminar carrier 101. By using a multi-conductive-layer carrier, rerouting of the lead positions may be accomplished. For example hidden package 105H by means of, if both packages are identical memory chips requiring

individual chip select signals, a chip select signal may be routed to an unused lead of the hidden IC package 105H, then routed within the carrier 101 to the proper location on the exposed IC package 105E. As all other signals may be shared in common, interconnections between leads of the hidden IC package 105H and identically corresponding leads of the exposed IC package 105E may be made by plated through-holes in the carrier 101. The circuit board 301 may incorporate one or more heat-sink layers 304 with which the bodies of hidden IC packages 104H are in surface-to-surface contact, either directly or indirectly via a thin layer of thermally-conductive paste, such as zinc oxide paste (not shown).

Referring now to Figure 4, surface mounting of the package units 201 on the circuit board 301 has resulted in a completed first embodiment module 401. A cross sectional view through the plane ABCD 402 provides the view of Figure 5.

A second embodiment of the invention, shown in Figures 6 through 10, utilizes a carrier 601 which has a pair of recesses 602 for back-to-back mounting of a pair of TSOP IC packages 105. The edges surrounding each recess 602 are equipped with an electrical contact pad set 603 to which the leads 104 of each IC package are electrically connected. The bodies 604 of two IC packages 105 may be in contact with opposite sides of a heat sink layer 605 embedded within the carrier substrate. A conductive paste (not shown) may be employed to enhance heat transfer between the package body 106 and the heat sink layer 605. The resulting assembly, shown in Figure 7, constitutes a second embodiment IC package unit 701.

Referring now to Figure 8, multiple second embodiment package units 701 (in this example, four) are shown ready for mounting on a circuit board 801. In this

example, two package units 701A and 701B will be mounted on the upper surface 802U of the circuit board 801, while two package units 701C and 701D will be mounted on the lower surface 802L thereof. Each package mounting location on the circuit board 801 has a set of board contact pads 803 to which the leads 104 of a hidden adjacent IC package 105H of each package unit 701 will be conductively bonded. The leads 104 of the exposed nonadjacent IC package 105E of each package unit 701 are coupled to the leads 104 of the hidden package 105H by means of connections which penetrate the 601. As is the case with the first embodiment of the invention, by using a multi-conductive-layer carrier, rerouting of the lead positions may be accomplished. For example, if both packages are identical memory chips requiring individual chip select signals, a chip select signal may be routed to an unused lead of the hidden IC package 105H, then routed within the carrier 601 to the proper location on the exposed IC package 105E. As all other signals may be shared in common, interconnections between leads of the hidden IC package 105H and identically corresponding leads of the exposed IC package 105E may be made by plated through-holes in the carrier 601.

Referring now to Figure 9, surface mounting of the package units 701 on the circuit board 801 has resulted in a completed second embodiment module 901. A cross sectional view of the module 901 through the plane EFGH 902 provides the view of Figure 10.

A third embodiment IC package unit, shown in Figures 11-14 is used for both third and fourth embodiment modules. The third embodiment package unit incorporates features of both the first and second embodiment package units 201 and

701, respectively. One of the pair of IC packages 105 is mounted on a planar surface of the carrier right-side up, while the other package is mounted within a recess on the opposite side of the carrier upside down. Using such a mounting configuration, both IC packages of each package unit are positioned as though stacked one on top of the other. For identical packages, interconnection of common signal lines is facilitated.

Referring now to Figures 11-14, the third embodiment package unit utilizes a carrier 1101 which has a planar first major surface 1102 and a second major surface 1103 with a package mounting recess 1104. Both the planar surface 1102 and the recess-equipped second surface 1103 have an electrical contact pad set 1105A and 1105B, respectively, to which the leads 104 of each IC package 105 are to be electrically connected. The body of the recessed IC package 105R may be in contact with a heat sink layer 1106 embedded within the carrier substrate 1107. A conductive paste (not shown) may be employed to enhance heat transfer between the package body and the heat sink layer 1106. The resulting assembly, shown in Figures 12 and 14, constitutes the third embodiment IC package unit 1201.

Referring now to Figure 15, multiple third embodiment package units 1201 (in this example, four) are shown ready for mounting on a circuit board 1501 having two major opposing planar surfaces on which package units may be mounted. In this example, two package units 1201A and 1201B will be mounted on the upper surface 1502U of a circuit board 1501, while two package units 1201C and 1201D will be mounted on the lower surface 1502L thereof. Each package mounting location on the circuit board 1201 has a set of board contact pads 1203 to which the leads 104 of a hidden adjacent IC package 105H of each package unit 1201 will be conductively

bonded. The leads 104 of the exposed nonadjacent IC package 105E of each package unit 1201 are coupled to the leads 104 of the hidden package 105H by means of connections which penetrate the carrier 1101. As is the case with the first and second embodiments of the invention, by using a multi-conductive-layer carrier, rerouting of the lead positions may be accomplished. For example, if both packages are identical memory chips requiring individual chip select signals, a chip select signal may be routed to an unused lead of the hidden IC package 105H, then routed within the carrier 1101 to the proper location on the exposed IC package 105E. As all other signals may be shared in common, interconnections between leads of the hidden IC package 105H and identically corresponding leads of the exposed IC package 105E may be made by plated through-holes in the carrier 1101.

Referring now to Figure 16, surface mounting of the package units 1201 on the circuit board 1501 has resulted in a completed third embodiment module 1601. A cross sectional view of the module 1601 through the plane IJKL 1602 provides the view of Figure 19.

Referring now to Figure 17, multiple third embodiment package units 1201 (in this example, four) are shown ready for mounting on a circuit board 1701 having two major opposing surfaces equipped with package unit mounting recesses 1702. In this example, two package units 1201A and 1201B will be mounted on the upper surface 1702U of a circuit board 1701, while two package units 1201C and 1201D will be mounted on the lower surface 1702L thereof. Each recessed mounting location on the circuit board 1701 has a set of board contact pads 1703 to which the leads 104 of a hidden adjacent IC package 105H of each package unit 1201A-1201D conductively

bonded. The leads 104 of the exposed nonadjacent IC package 105E of each package unit 1201A-1201D are coupled to the leads 104 of the hidden package 105H by means of connections which penetrate the carrier 1101. As is the case with the first and second embodiments of the invention, by using a multi-conductive-layer carrier, rerouting of the lead positions may be accomplished. For example, if both packages are identical memory chips requiring individual chip select signals, a chip select signal may be routed to an unused lead of the hidden IC package 105H, then routed within the carrier 1101 to the proper location on the exposed IC package 105E. As all other signals may be shared in common, interconnections between leads of the hidden IC package 105H and identically corresponding leads of the exposed IC package 105E may be made by plated through-holes in the carrier 1101.

Referring now to Figure 18, surface mounting of the package units 1201 on the circuit board 1701 has resulted in a completed fourth embodiment module 1801. A cross sectional view of the module 1801 through the plane MNOP 1802 provides the view of Figure 20.

A fourth embodiment IC package unit, shown in Figures 21-24 is used for a fifth embodiment module. Referring now to Figure 21, the primary difference between the fourth embodiment carrier 2101 and that of the third embodiment carrier 1101 is the addition of carrier leads 2108, which are used to attach the fourth embodiment package unit to a circuit board. The fourth embodiment carrier 2101 also has a planar first major surface 2102 and a second major surface 2103 with a package mounting recess 2104. Both the planar surface 2102 and the recess-equipped second surface 2103 have an electrical contact pad set 2105A and 2105B, respectively, to which the leads 104 of

each IC package 105 are to be electrically connected. The body 106 of the recessed IC package 105R may be in contact with a heat sink layer 2106 embedded within the carrier substrate 2107. A conductive paste (not shown) may be employed to enhance heat transfer between the package body and the heat sink layer 2106. The resulting assembly, shown in Figures 22 and 24, constitutes the fourth embodiment IC package unit 2201. Each of the IC packages 105 of a package unit is mounted in a stacked relationship, which means that corresponding leads on two identical IC packages lie directly above and below one another. Such a configuration facilitates interconnection of the common pins on both chips, as plated through-hole connectors can be used without rerouting traces within the carrier substrate 2107.

Referring now to Figure 25, multiple fourth embodiment package units 2201 (in this example, four) are shown ready for mounting on a circuit board 2501 having two major opposing planar surfaces on which package units may be mounted. In this example, two package units 2201A and 2201B will be mounted on the upper surface 2502U of a circuit board 2501, while two package units 2201C and 2201D will be mounted on the lower surface 2502L thereof. Each package mounting location on the circuit board 2501 has a set of board contact pads 2503 to which the carrier leads 2108 of each package unit 2201 will be conductively bonded.

Referring now to Figure 26, surface mounting of the package units 2201 on the circuit board 2501 has resulted in a completed fifth embodiment module 2601.

Referring now to Figures 27 and 28, a fifth embodiment IC package unit is constructed using a thin film carrier substrate 2701. Other than this distinctive feature, the resulting sixth embodiment package unit 2801 is functionally identical to the first

embodiment package unit 201.

Referring now to Figure 29, a seventh embodiment electronic module utilizes a sixth embodiment carrier 2901 designed for the mounting of multiple ball-grid array IC packages 2902. Such packages employ pads, rather than leads, to make connection from a semiconductor chip to the external world. This carrier 2901 incorporates butt-I-joint leads 2903, which are solder reflowable for mounting to pads on a printed circuit board. Each of the ball-grid array IC packages 2902 has a plurality of connection elements, which in this case are pads, 2904 on each of which a metal (e.g., gold) ball 2905 has been bonded or solder reflow attached. Referring now to Figure 30, each of the ball-grid array IC packages 2902 has been mounted on the carrier 2901 and each of the balls 2905 is physically and electrically bonded to a corresponding pad 2906 on the carrier 2901. Bonding can be via solder reflow, via vibrational energy input, or any other known technique. The mounting process has created a multiple-package ball-grid array package unit 3001.

Referring now to Figure 31, each of the butt-I-joint leads 2903 of carrier 2901 has been solder reflowed to a pad 3101 on printed circuit board 3102, thereby interconnecting the ball-grid array package unit 3001 to the board circuitry (not shown). Figure 32 shows eight of such package units 3001 mounted on a printed circuit board 3201 of the type known as a DIMM module. DIMM modules are in wide use as SDRAM memory modules for personal computers.

Referring now to Figure 33, a ball-grid array IC package unit 3300 having only two ball-grid-array packages 3301 thereon is shown. Figure 34 shows this IC package unit 3300 mounted on a portion of a circuit board 3401.

Although only several embodiments of the present invention have been disclosed and described herein, it will be obvious to those having ordinary skill in the art of semiconductor assembly technology, that changes and modifications may be made thereto without departing from the scope of the invention as hereinafter claimed. For example, the types of leads shown in for the various IC packages and carriers are those which are in common usage at the time of the filing of the application. Other leads having similar, but more compact, features have been developed and will likely come into common usage.

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CLAIMS

What is claimed is:

1 1. An electronic circuit module comprising:

2       at least one IC package unit, each unit having

3            a carrier having first and second IC package mounting locations on

4       opposed sides thereof, said first mounting location having a first mounting pad array,

5       said second mounting location having a second mounting pad array, said first and

6       second mounting arrays being coupled to a carrier interface; and

7            a pair of IC packages, each package having a package body containing

8           an integrated circuit chip and a plurality of connection elements coupled to said chip

9           and extending at least to the surface of said body, the connection elements of said first

10       package being conductively bonded to said first mounting pad array, the connection

11       elements of said second package being conductively bonded to said second mounting

12       pad array; and

13            a printed circuit board having at least one interconnection pad array affixed

14       thereto, each interconnection pad array coupled to circuitry on the printed circuit board

15       and conductively bonded to the interface of a single IC package unit.

1 2. The electronic circuit module of claim 1, wherein individual mounting pads of said

2       first mounting pad array are coupled to individual mounting pads of said second

3       mounting pad array by means of conductive links within the carrier, and the leads of

4       one of said IC packages are conductively bonded directly to said interconnection pad

5 array.

1 3. The electronic circuit module of claim 1, wherein said carrier comprises a flexible  
2 polymeric film having first and second major planar faces corresponding, respectively,  
3 to said first and second IC package mounting locations.

1 4. The electronic circuit module of claim 3, wherein said circuit board includes a  
2 recess for each package unit affixed thereto, said recess receiving at least a portion of  
3 the body of one of said packages.

5. The electronic circuit module of claim 1, wherein said carrier comprises a semi-  
rigid laminar substrate having first and second major faces corresponding, respectively,  
to said first and second IC package mounting locations.

6. The electronic circuit module of claim 5, wherein said circuit board includes a  
recess for each package unit affixed thereto, said recess receiving at least a portion of  
the body of one of said packages.

7. The electronic circuit module of claim 5, wherein said carrier further comprises a  
plurality of carrier leads, and individual mounting pads of said first mounting pad array  
and of said second mounting pad array are conductively coupled to individual carrier  
leads, said carrier leads being conductively bonded directly to said interconnection pad  
array.

6       8.     The electronic circuit module of claim 7, wherein said carrier leads are L-shaped  
7     and butt-soldered to the pads of the interconnection pad array.

1       9.     The electronic circuit module of claim 7, wherein said carrier leads are gullwing  
2     shaped.

1       10.    The electronic circuit module of claim 5, wherein each of said first and second  
2     major faces incorporates a recess for receiving a single IC package.

1       11.    The electronic circuit module of claim 5, wherein said first major face is planar,  
2     and said second major face incorporates a recess, said first IC package is mounted on  
3     said planar first major face and said second IC package is mounted within said recess.

1       12.    The electronic module of claim 1, wherein each IC package is of the ball-grid  
2     array type.

1       13.    An electronic circuit module comprising:  
2               at least one pair of IC packages, each package having a package body, an  
3               integrated circuit chip embedded within said body, and a plurality of connection  
4               elements coupled to said chip which extend at least to the surface of said body;  
5               one package carrier for each IC package pair, each carrier having two  
6               opposing major faces, each face having a mounting pad array to which the connection  
7               elements of one IC package of each package pair are conductively bonded, each

8 carrier having an interface coupled to the connection elements of both IC packages;

9 and

10 a printed circuit board having at least one interconnection pad array affixed  
11 thereto, each interconnection pad array conductively bonded to the carrier interface.

1 14. The electronic circuit module of claim 13, wherein pairs of mounting pads on  
2 opposite major faces of said package carrier are electrically interconnected, and the  
3 connection elements of one of said IC packages are conductively bonded directly to  
4 said interconnection pad array.

15. The electronic circuit module of claim 13, wherein said carrier comprises a flexible polymeric film, and said opposing major faces are planar.

16. The electronic circuit module of claim 13, wherein said main circuit board includes a recess for each package unit affixed thereto, said recess receiving at least a portion of the body of one of said packages.

1 17. The electronic circuit module of claim 13, wherein said carrier comprises a semi-  
2 rigid laminar substrate.

1       18. The electronic circuit module of claim 17, wherein said circuit board includes a  
2       recess for each package unit affixed thereto, said recess receiving at least a portion of  
3       the body of one of said packages.

4 19. The electronic circuit module of claim 17, wherein said carrier further comprises  
5 a plurality of carrier leads, and individual mounting pads of each mounting pad array are  
6 conductively coupled to individual carrier leads, said carrier leads being conductively  
7 bonded directly to said interconnection pad array.

1 20. The electronic circuit module of claim 19, wherein said carrier leads are gullwing  
2 shaped.

1 21. The electronic circuit module of claim 19, wherein said carrier leads are L-  
2 shaped, each lead being butt-soldered to a pad of the interconnection pad array.

1 22. The electronic circuit module of claim 17, wherein each of said opposing major  
2 faces incorporates a recess for receiving a single IC package.

1 23. The electronic circuit module of claim 17, wherein one of said major faces is  
2 planar, while the opposing major face incorporates a recess, one IC package of each  
3 package pair being mounted on said planar major face and the recess receiving at least  
4 a portion of the body of the other IC package of that pair.

1 24. An electronic circuit module comprising:  
2 an IC package unit having  
3 a plurality of IC packages, each package having a package body, an  
4 integrated circuit chip embedded within said body, and a plurality of connection

5 elements coupled to said chip which extend at least to the surface of said body;  
6 a package carrier having two opposing major faces, each face having at least  
7 one mounting pad array to which the connection elements of one IC package are  
8 conductively bonded, each carrier providing a carrier interface coupled to the  
9 connection elements of the IC packages on that carrier; and  
10 a printed circuit board having at least one interconnection pad array affixed  
11 thereto, each interconnection pad array conductively bonded to the carrier interface.

1 25. The electronic circuit module of claim 24, wherein pairs of mounting pads on  
2 opposite major faces of said package carrier are electrically interconnected, and the  
3 connection elements of one of said IC packages are conductively bonded directly to  
4 said interconnection pad array.

1 26. The electronic circuit module of claim 24, wherein said carrier comprises a  
2 flexible polymeric film, and said opposing major faces are planar.

1 27. The electronic circuit module of claim 24, wherein said main circuit board  
2 includes a recess for each package unit affixed thereto, said recess receiving at least a  
3 portion of the body of one of said packages.

1 28. The electronic circuit module of claim 24, wherein said carrier comprises a semi-  
2 rigid laminar substrate.

3 29. The electronic circuit module of claim 28, wherein said circuit board includes a

4      recess for each package unit affixed thereto, said recess receiving at least a portion of  
5      the body of one of said packages.

1      30.     The electronic circuit module of claim 28, wherein said carrier further comprises  
2      a plurality of carrier leads, and individual mounting pads of each mounting pad array are  
3      conductively coupled to individual carrier leads, said carrier leads being conductively  
4      bonded directly to said interconnection pad array.

1      31.     The electronic circuit module of claim 30, wherein said carrier leads are gullwing  
2      shaped.

3      32.     The electronic circuit module of claim 30, wherein said carrier leads are L-  
4      shaped, each lead being butt-soldered to a pad of the interconnection pad array.

1      33.     The electronic circuit module of claim 24, wherein each of said opposing major  
2      faces incorporates a recess for receiving a single IC package.

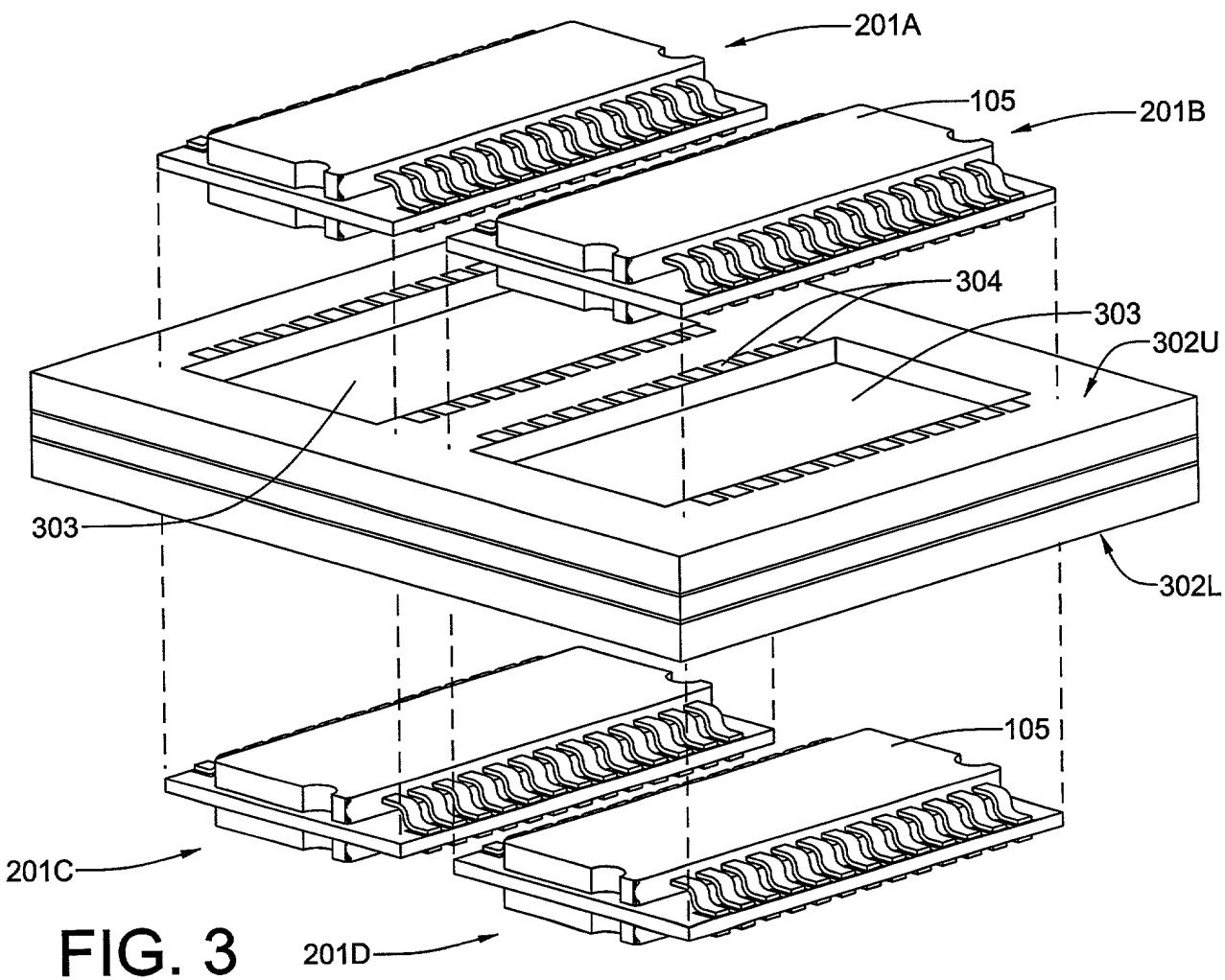
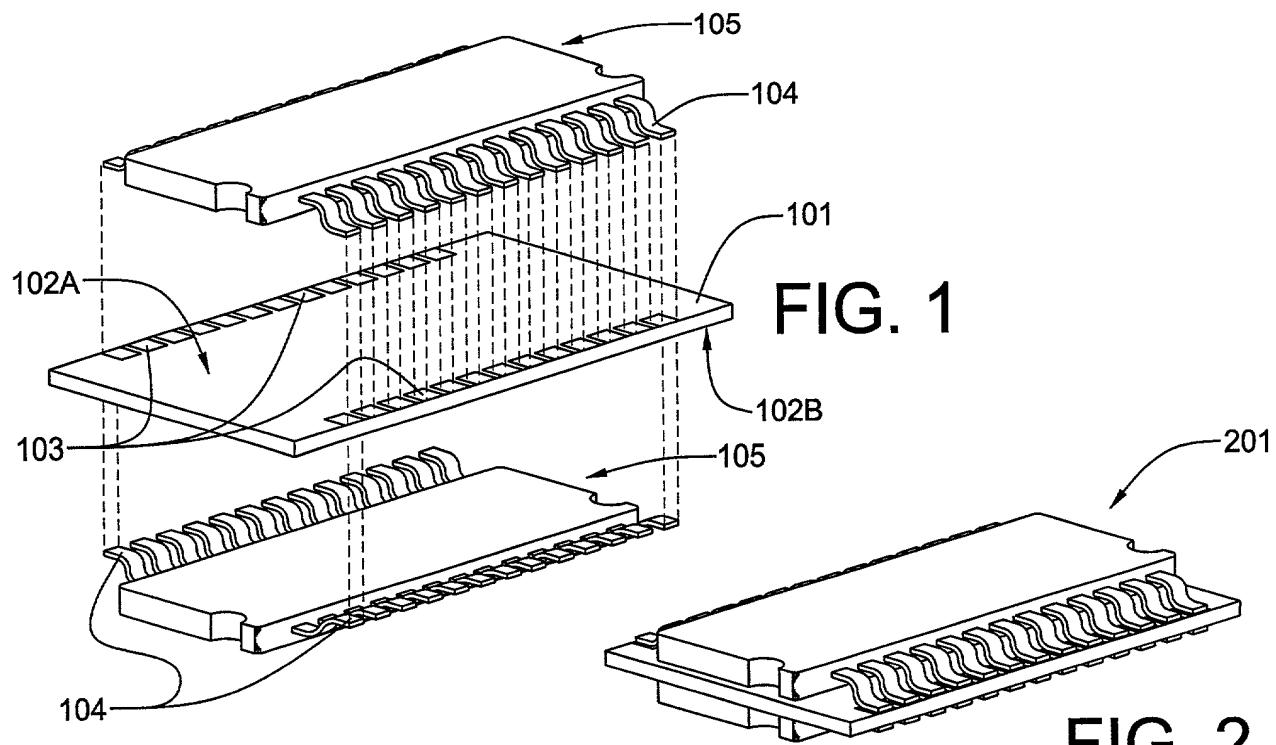
1      34.     The electronic circuit module of claim 24, wherein one of said major faces is  
2      planar, while the opposing major face incorporates at least one recess, at least one IC  
3      package being mounted on said planar major face and each recess receiving at least a  
4      portion of the body of an IC package.

## CARRIER-BASED ELECTRONIC MODULE

### ABSTRACT

An improved multi-chip module includes a circuit board having an array of electrical interconnection pads to which are mounted a plurality of IC package units. Each IC package unit includes multiple IC packages, which are mounted on opposite sides of a package carrier. The package units may be mounted on one or both sides of the circuit board. A variety of package carriers are used to create a number of different modules. One type of package carrier has a pair of major planar surfaces. Each planar surface incorporates electrical contact pads. At least one IC package is surface mounted on each major planar surface, by interconnecting the connection elements, or leads, of the package with the contact pads on the planar surface, to form the IC package unit. Another type of package carrier substrate has a multiple recesses for back-to-back surface mounting of the IC packages. The IC packages may be in contact with opposite sides of a heat sink layer embedded within the carrier substrate. Each resulting IC package unit is surface mounted to the circuit board. Still another type of package carrier combines features of the first two carriers. At least one of the packages is mounted on a planar surface of the carrier right-side up, while at least one other package is mounted on the carrier in a recess upside down. Two module types are shown using such a carrier. Any of the carriers may be equipped with its own set of interconnection leads or connection may be made directly between the leads of one package and the interconnection pads of the circuit board. Thin-film carriers may be employed in the construction of package modules, as may be ball-grid-array type packages.

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10  
15  
20



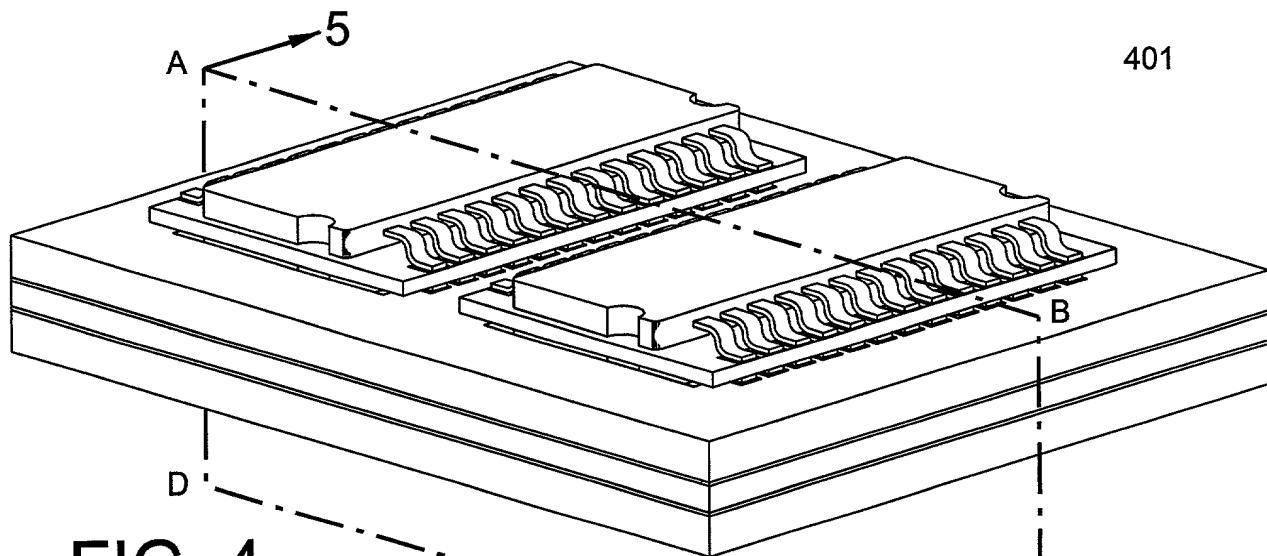


FIG. 4

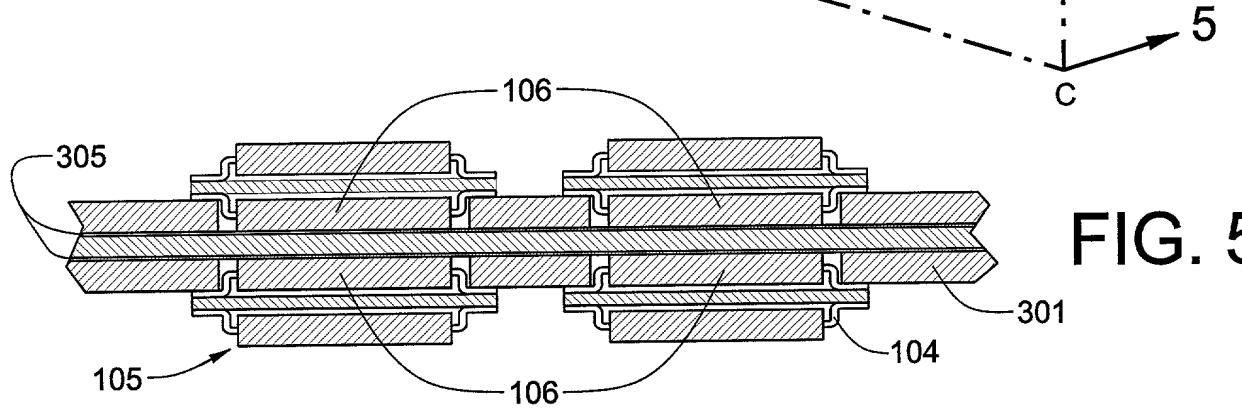


FIG. 5

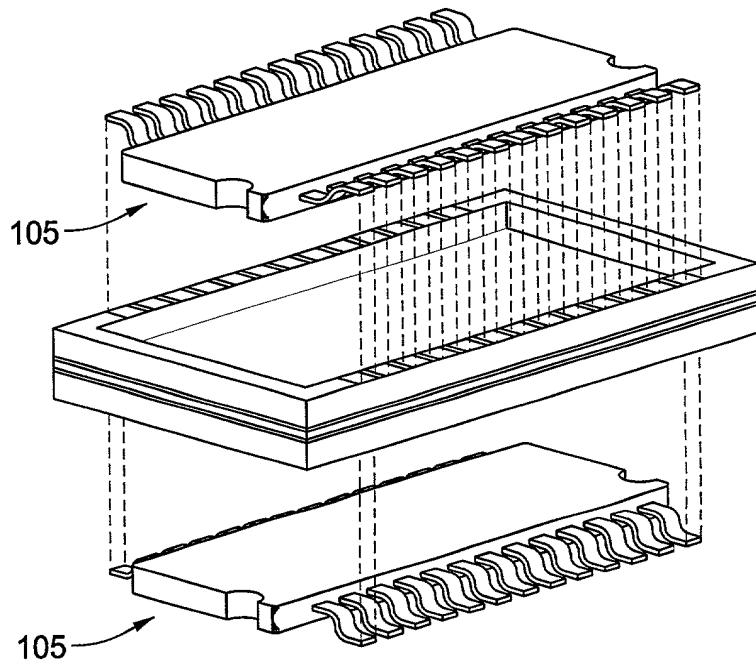
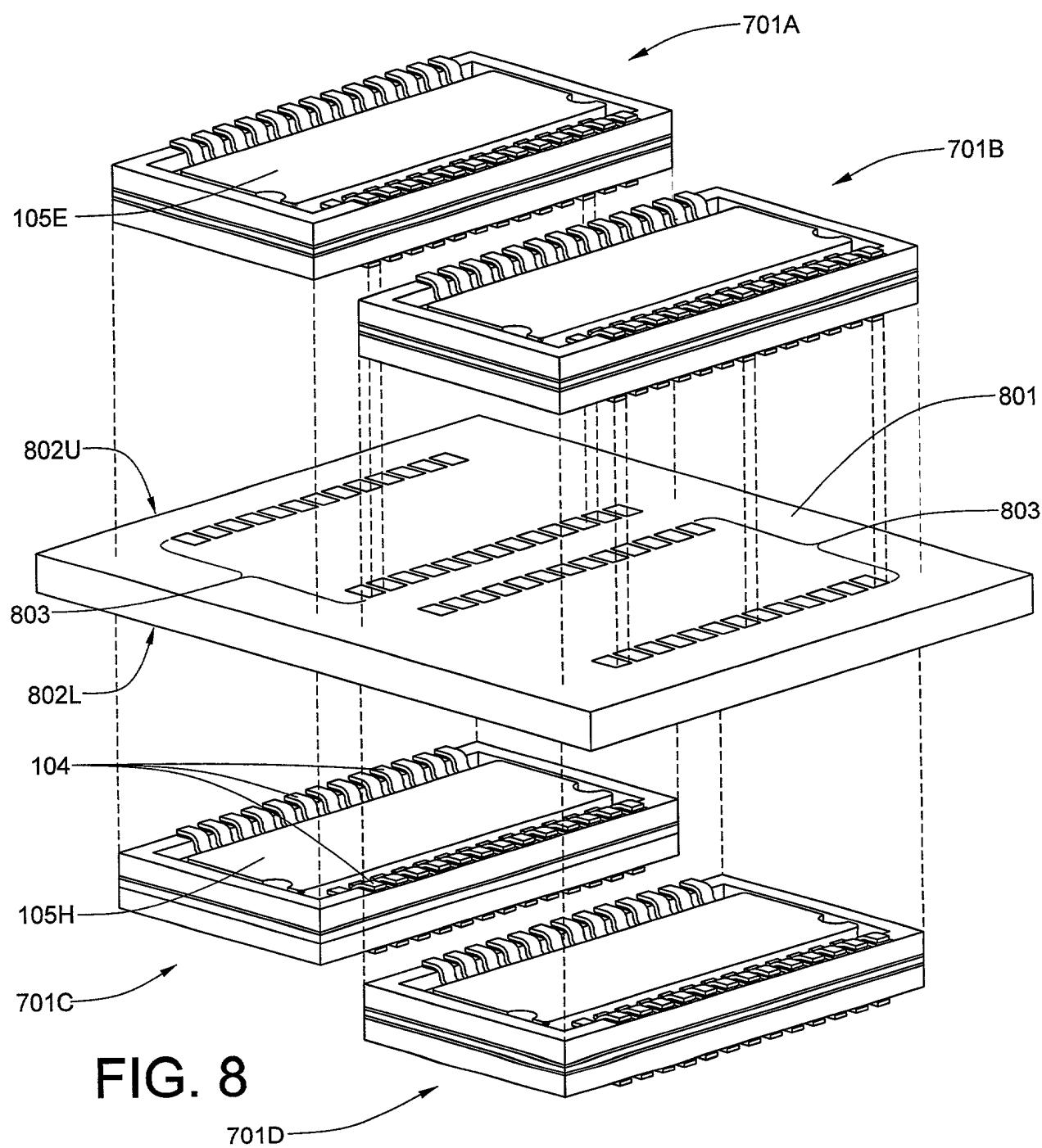
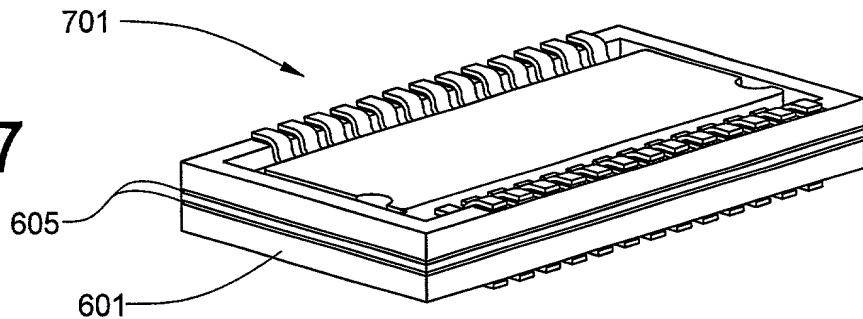


FIG. 6

**FIG. 7****FIG. 8**

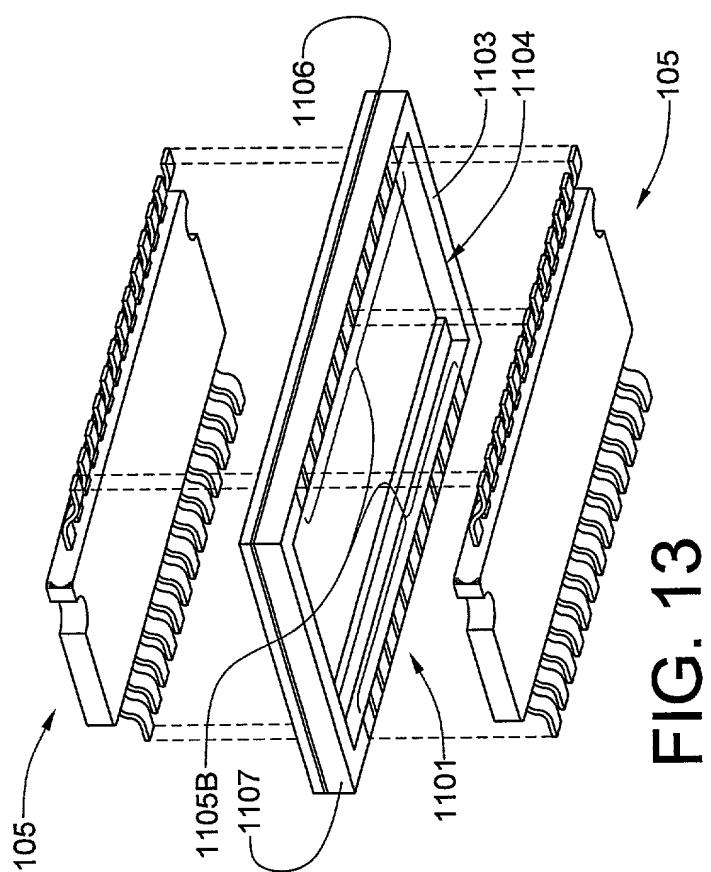


FIG. 13

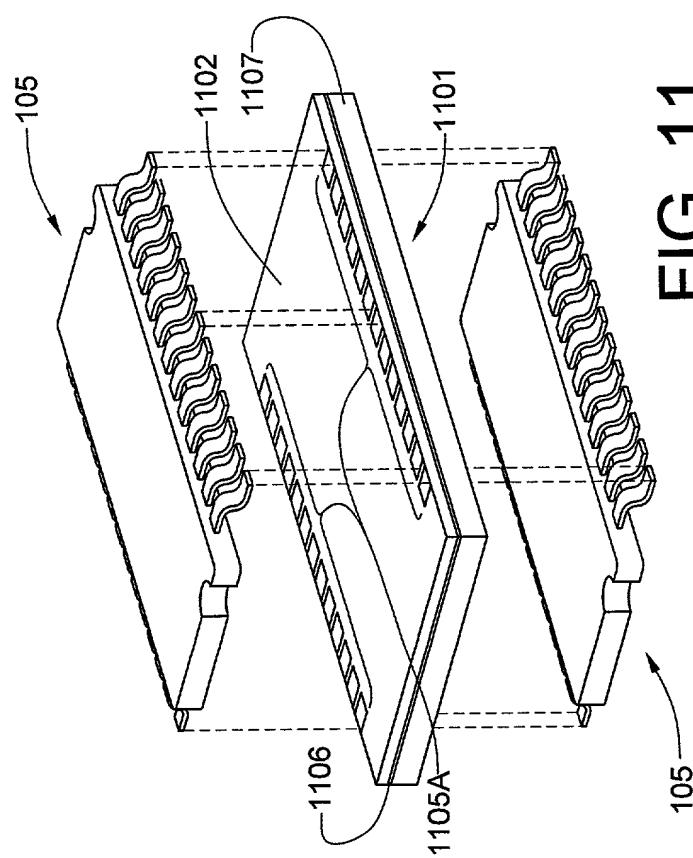


FIG. 11

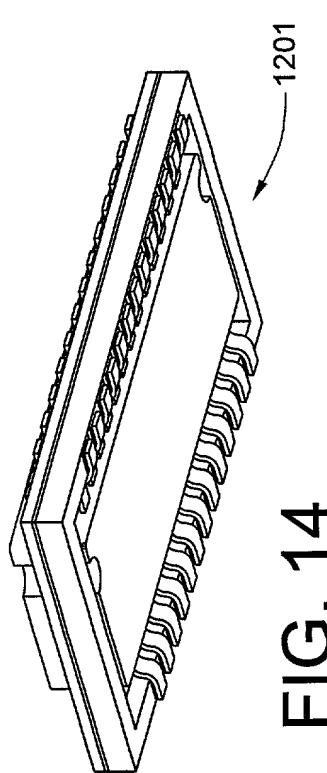


FIG. 14

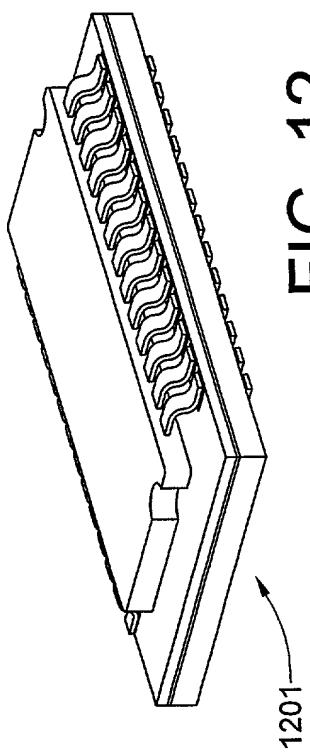


FIG. 12

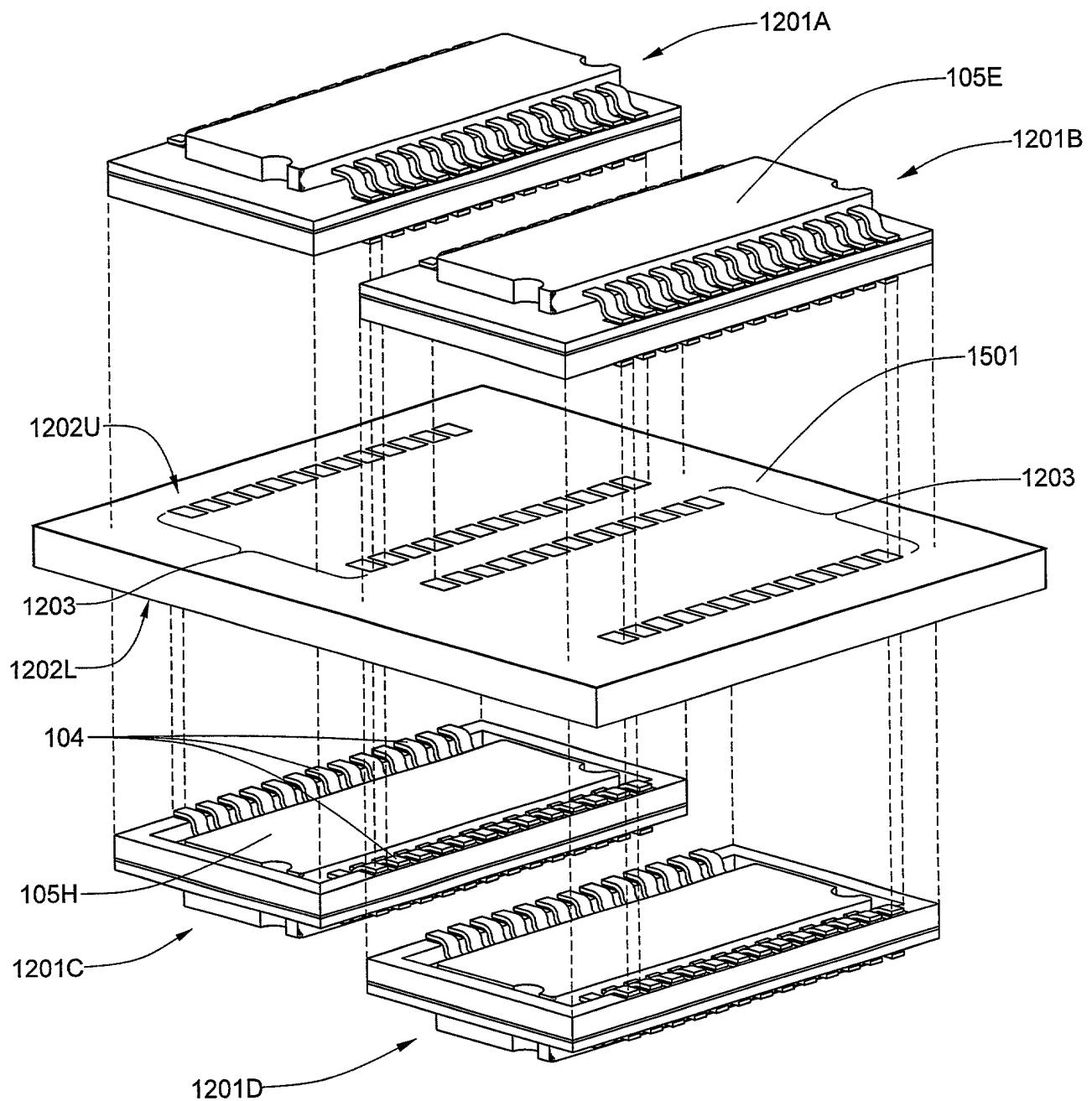
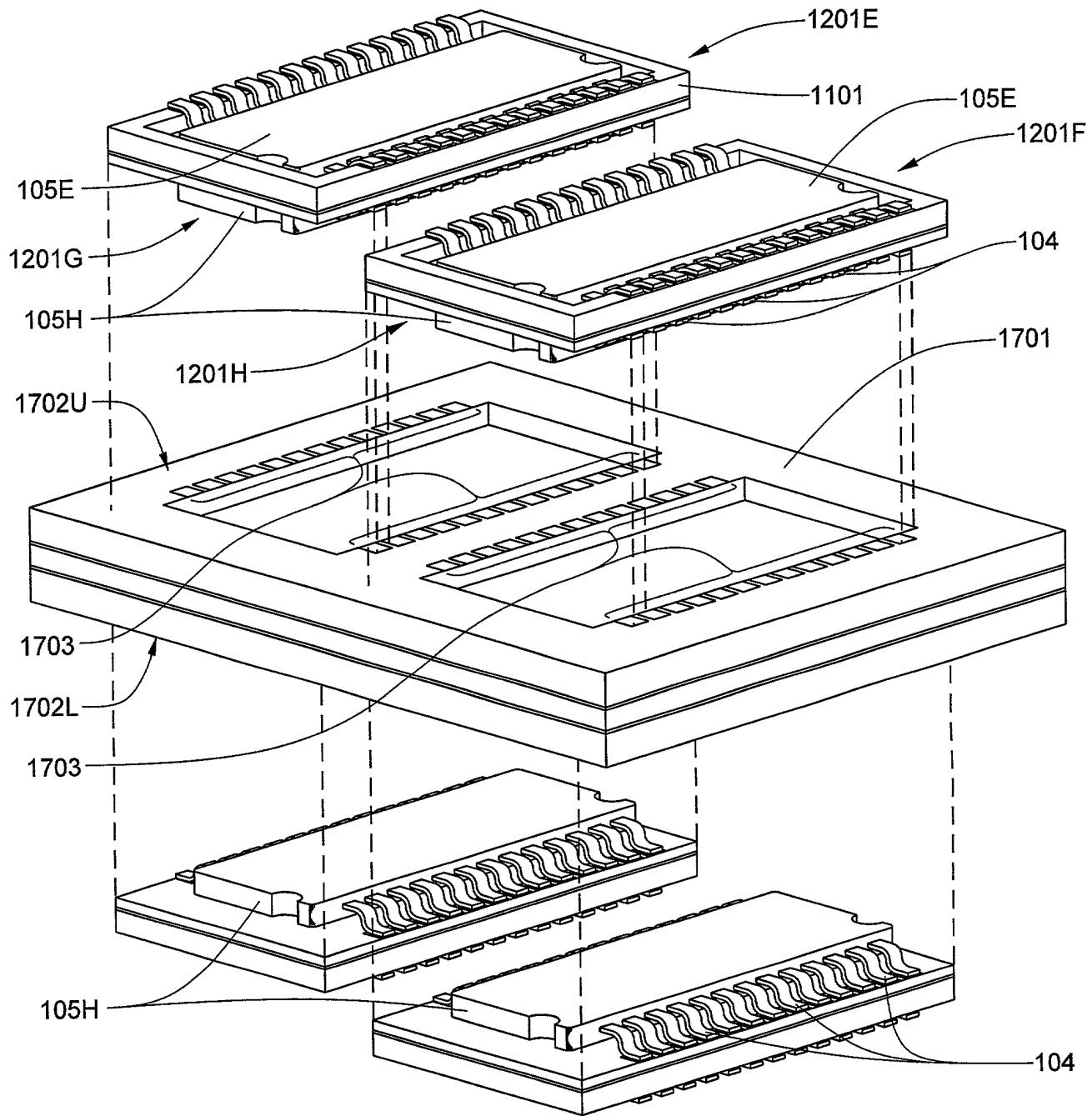
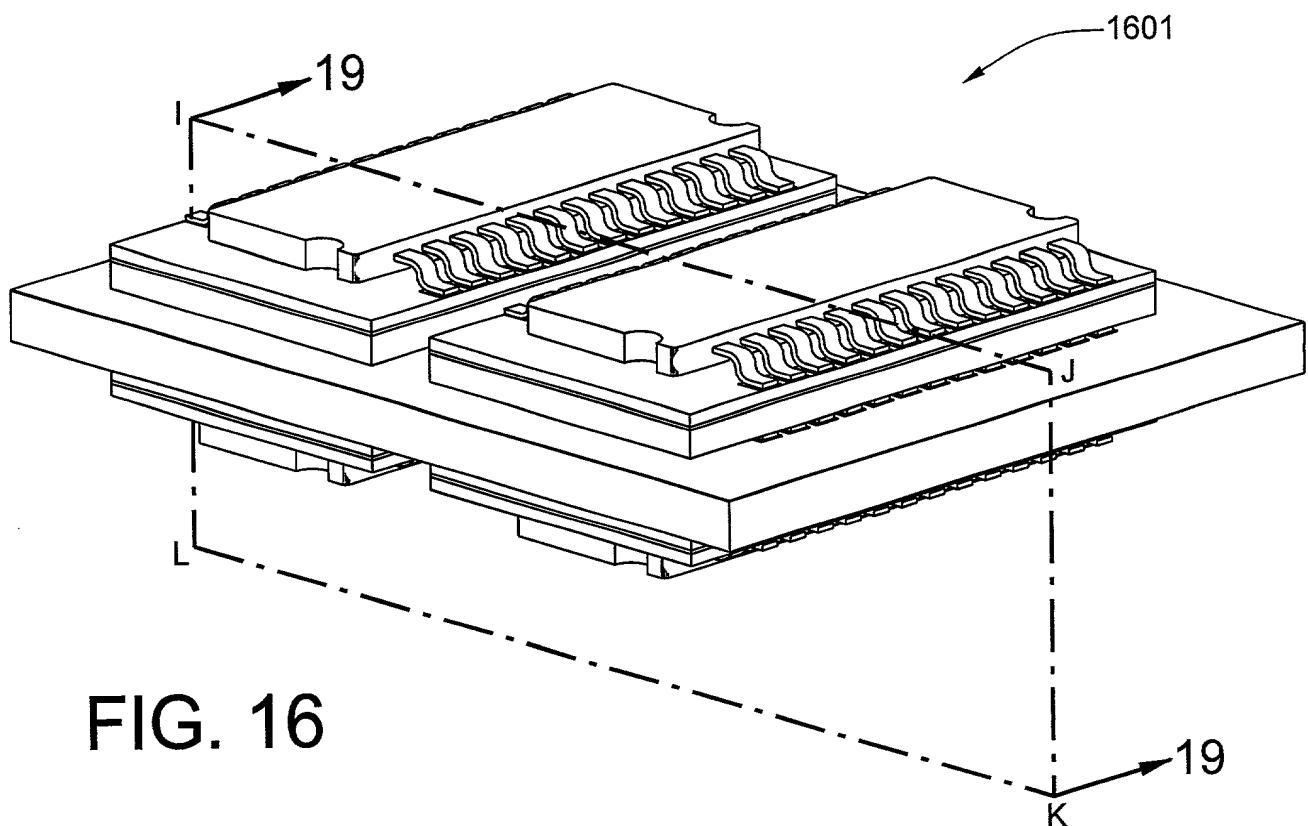


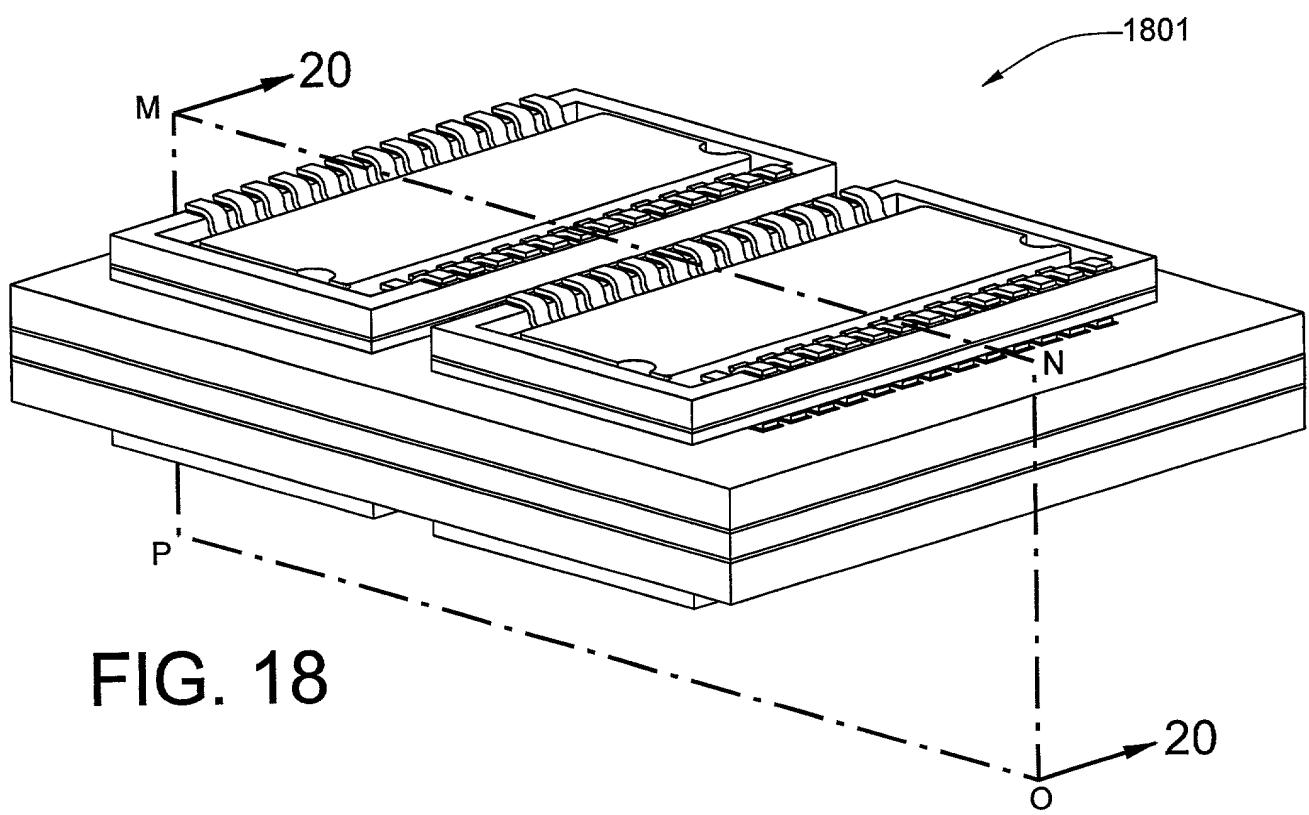
FIG. 15



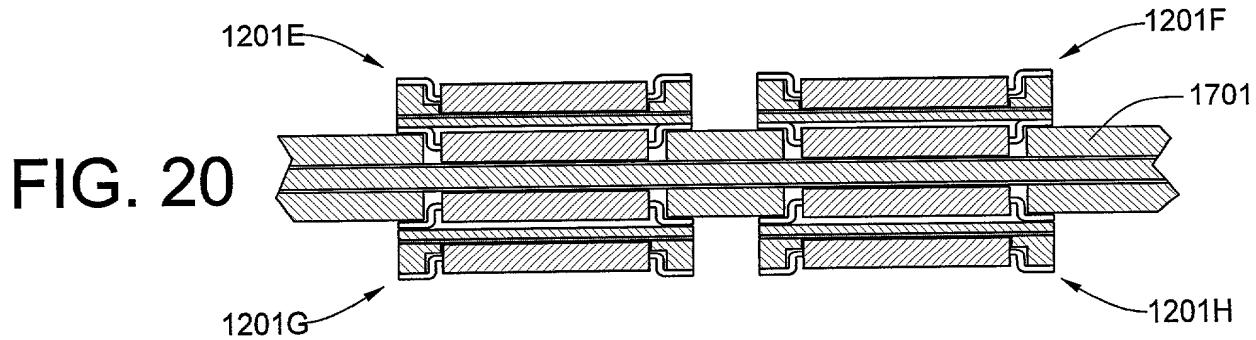
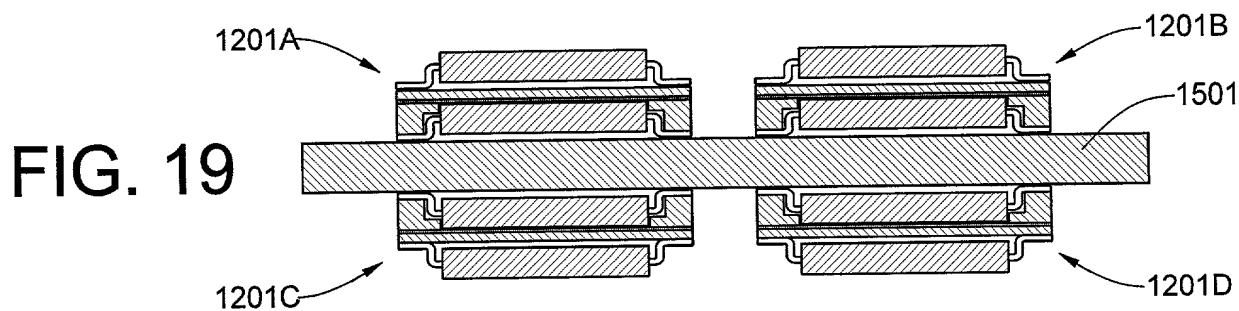
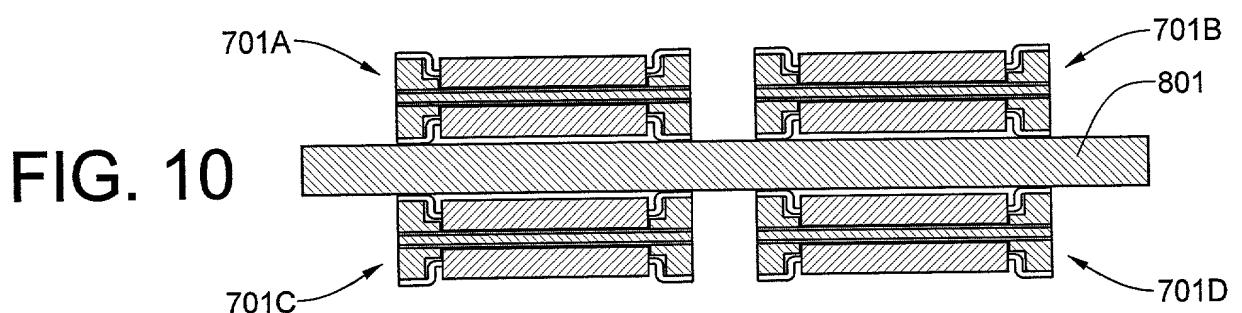
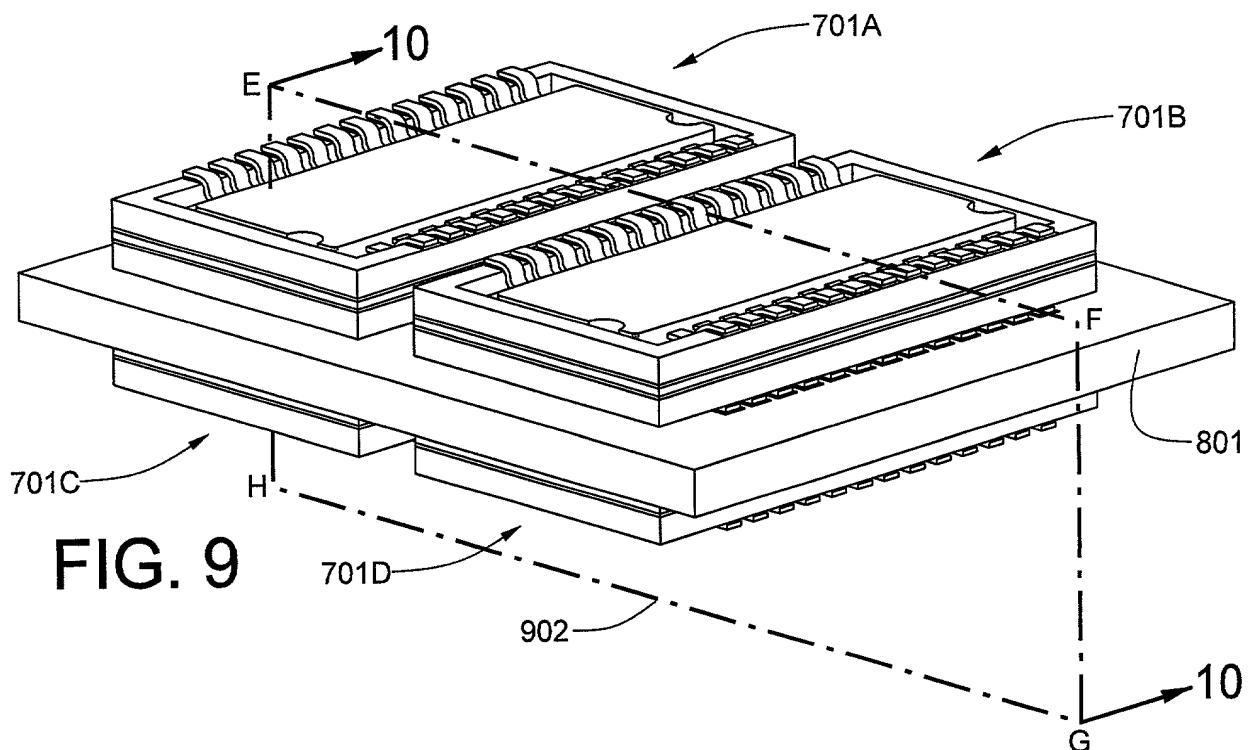
**FIG. 17**



**FIG. 16**



**FIG. 18**



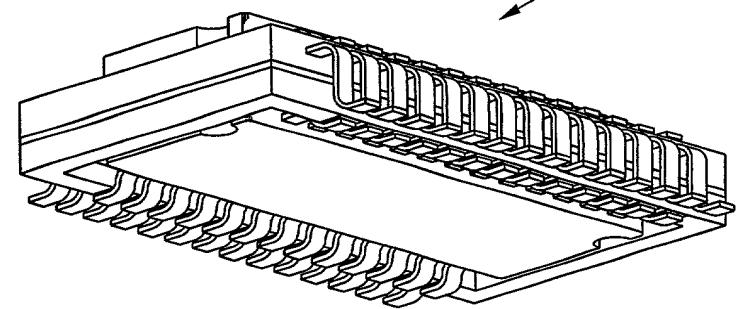
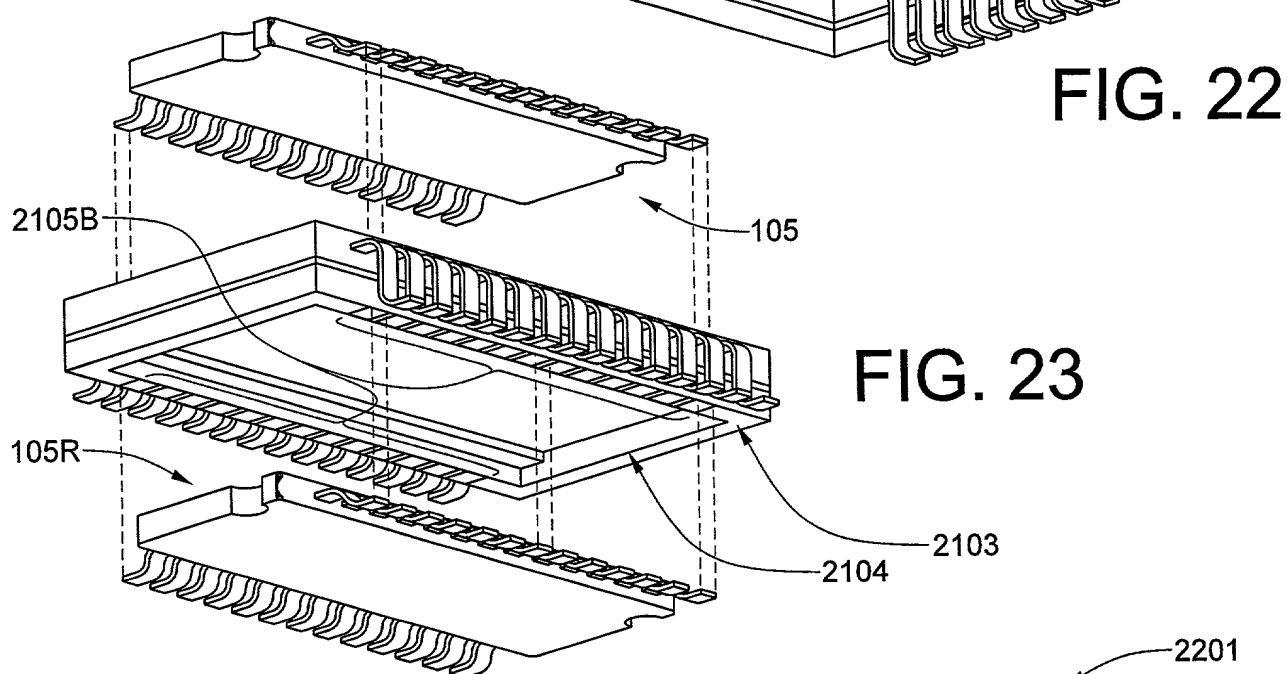
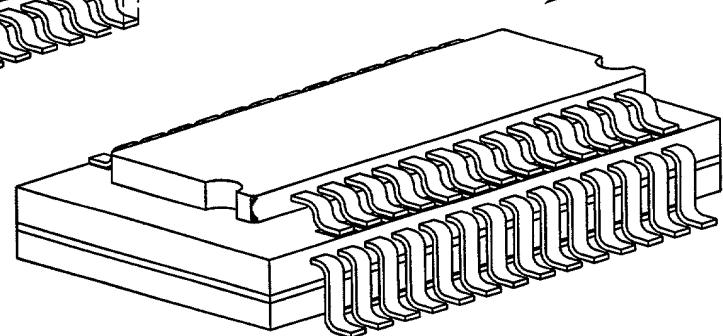
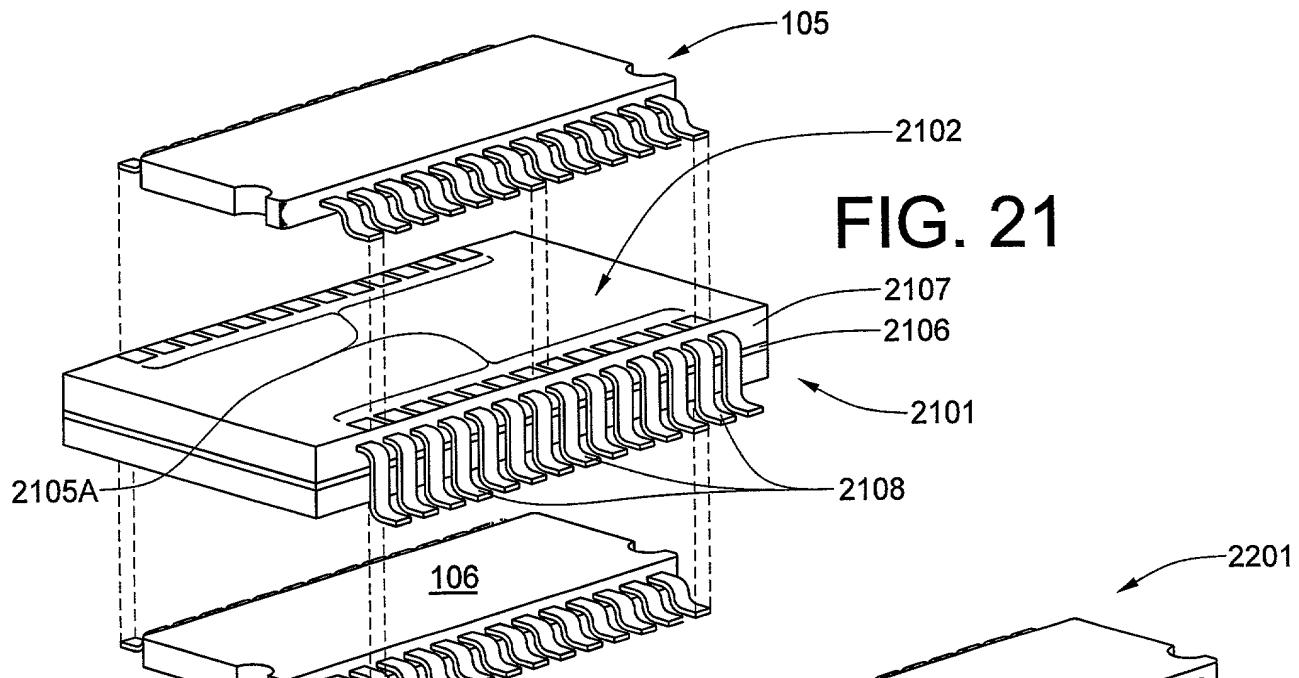
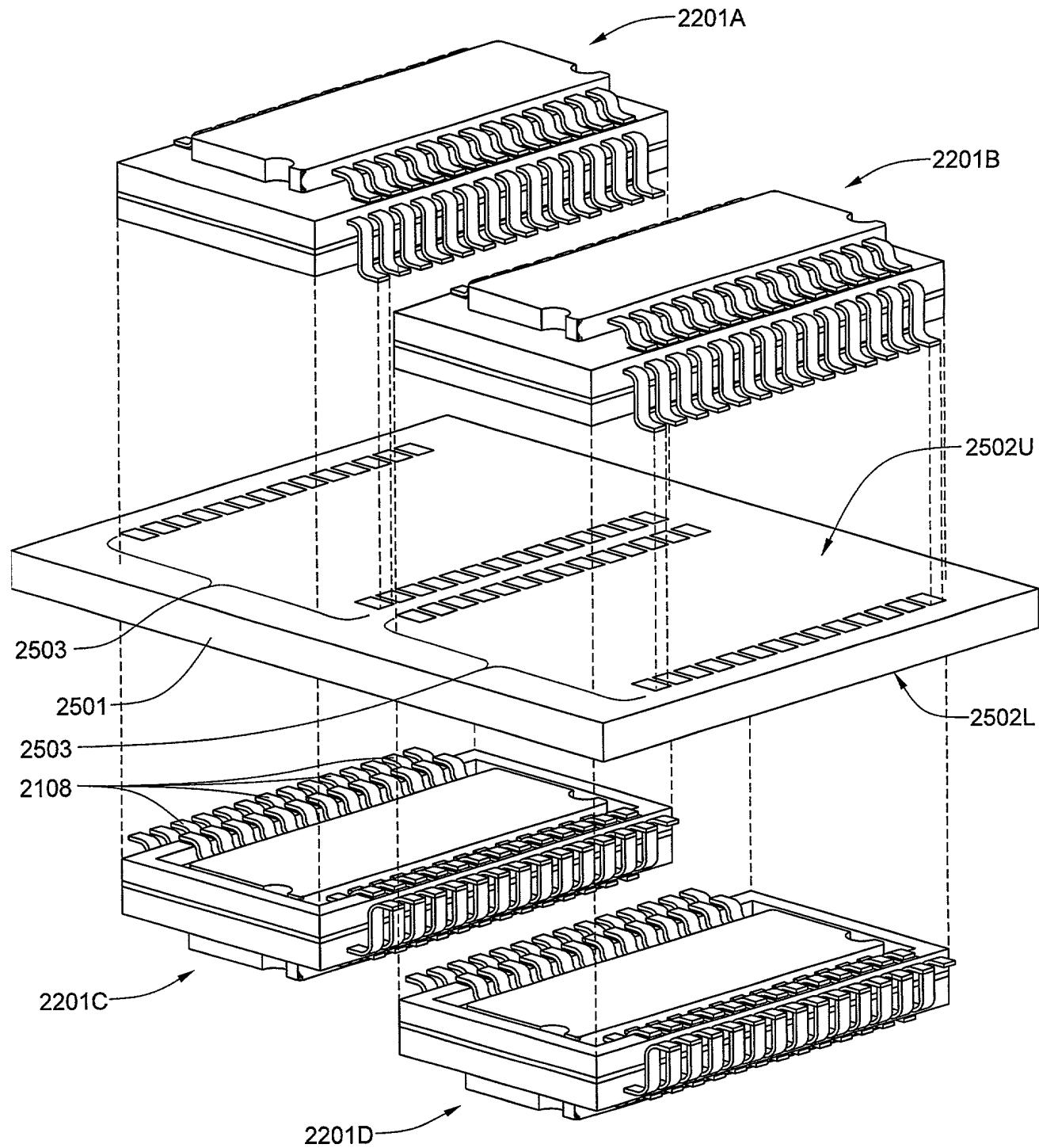


FIG. 24



**FIG. 25**

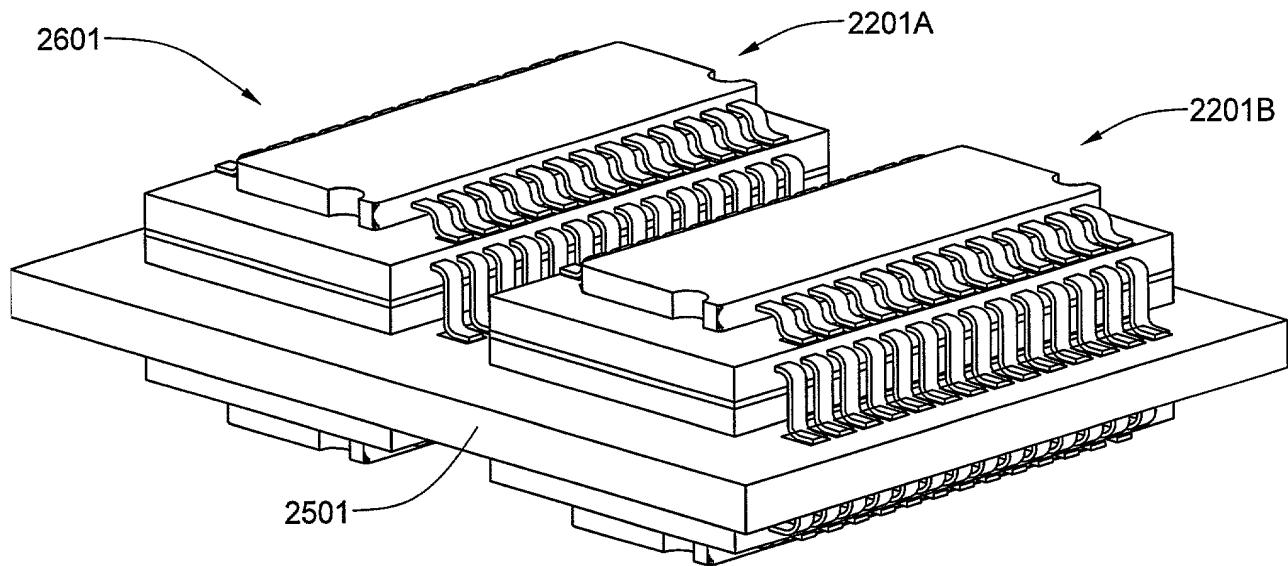


FIG. 26

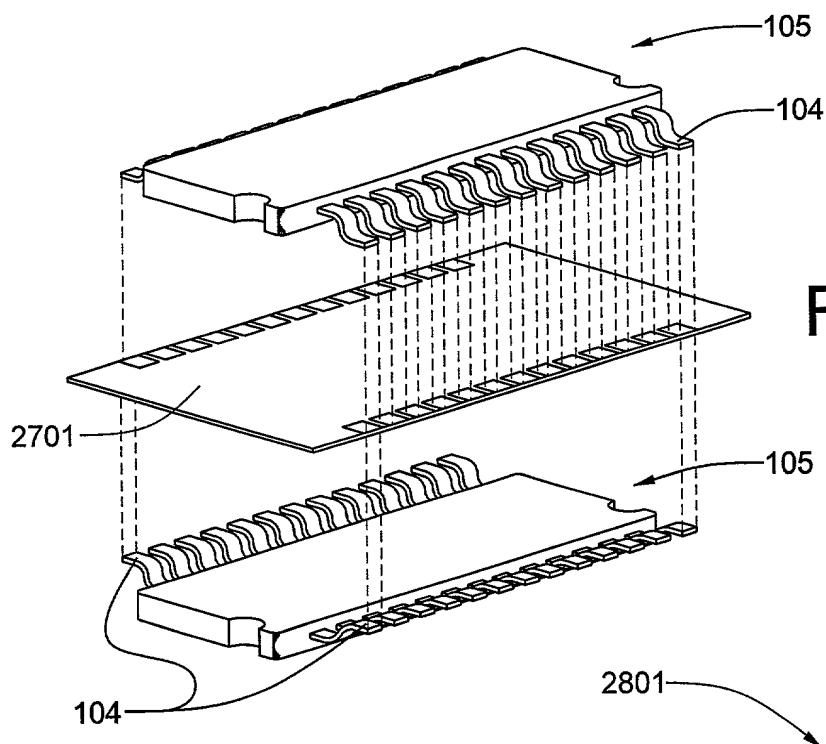
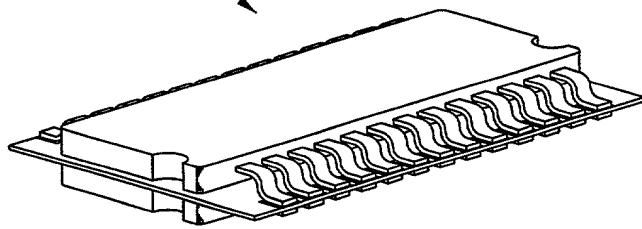
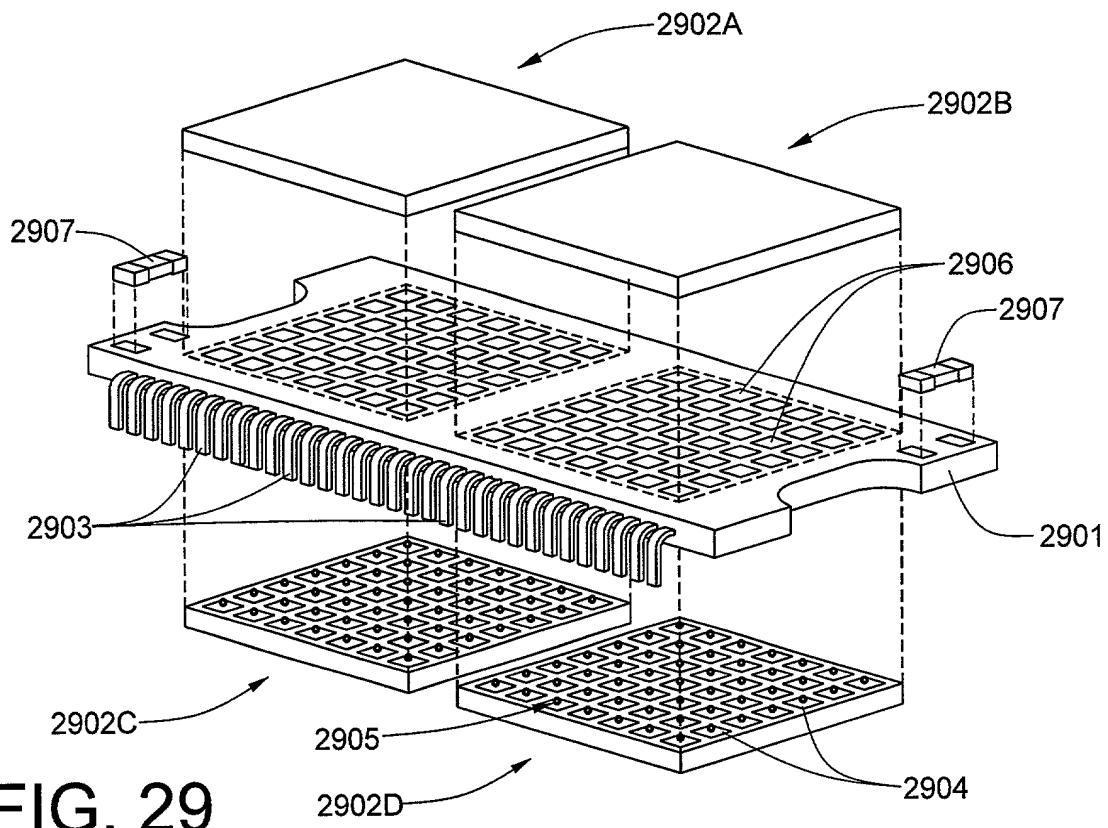


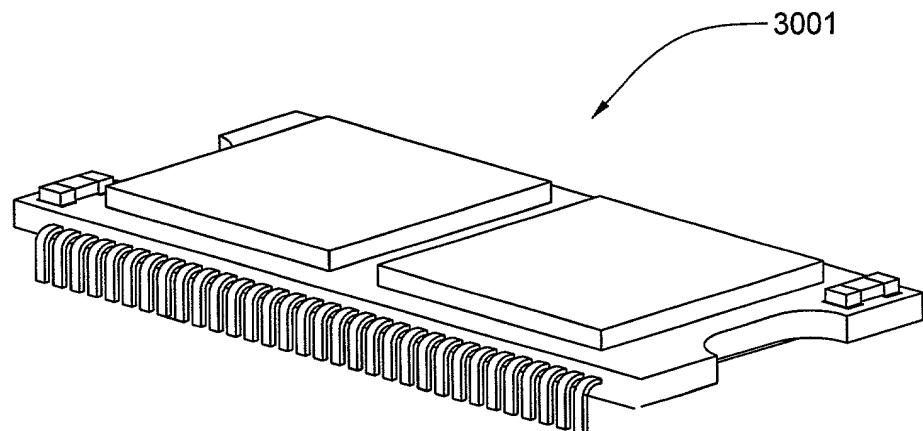
FIG. 27





**FIG. 29**

00136500-1001600



**FIG. 30**

003707005200

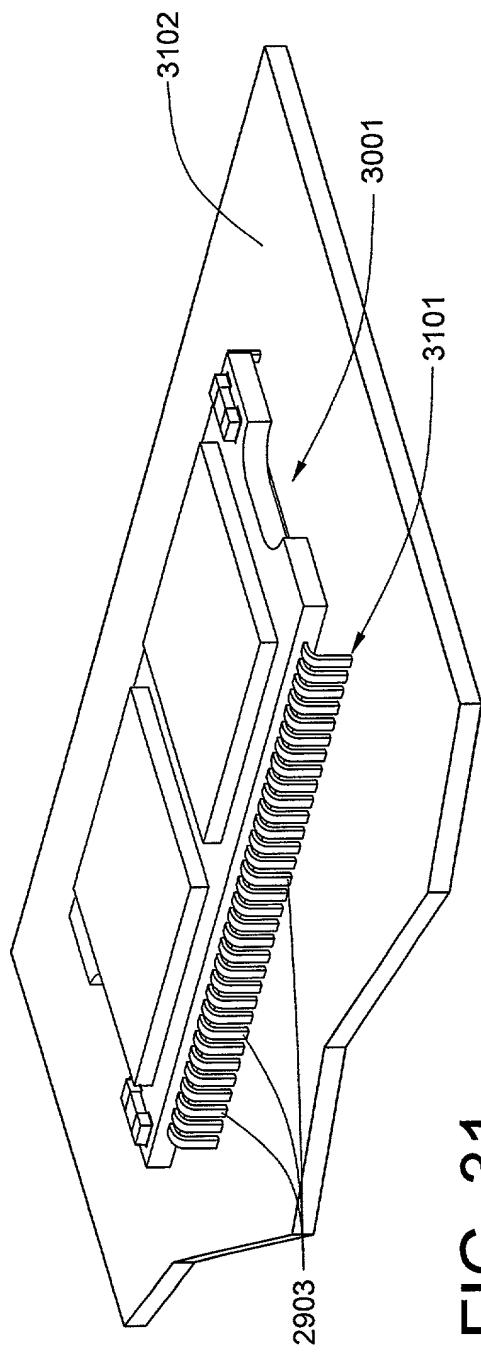


FIG. 31

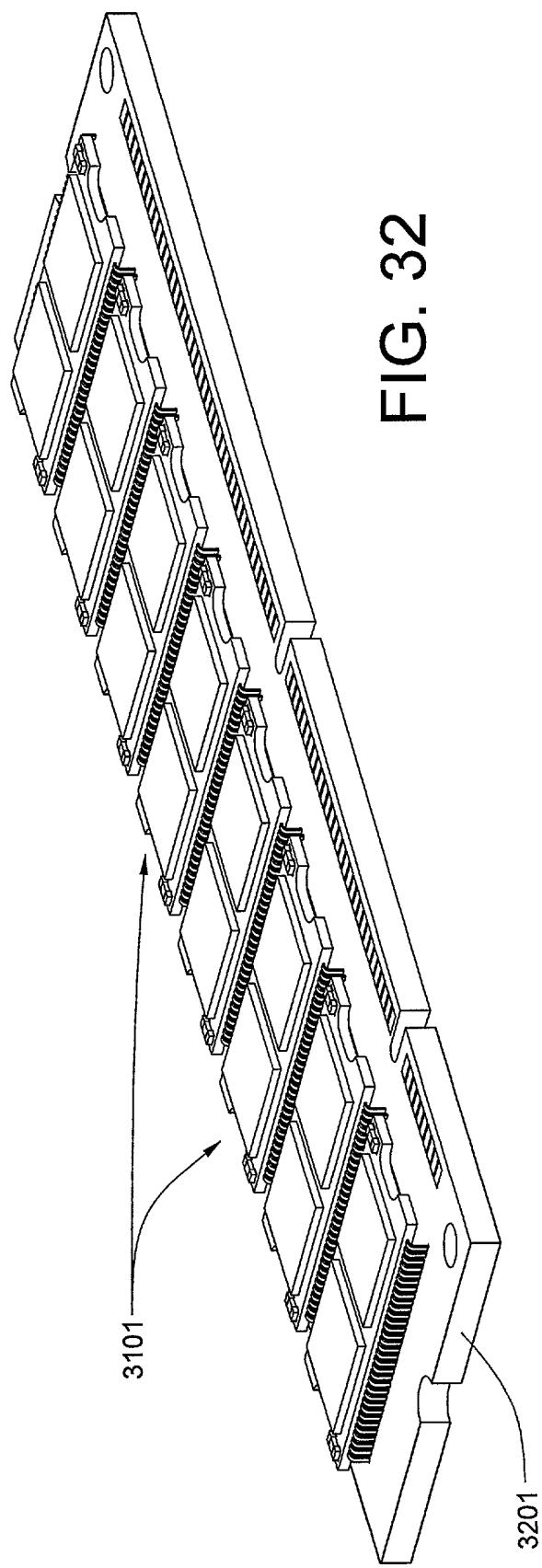
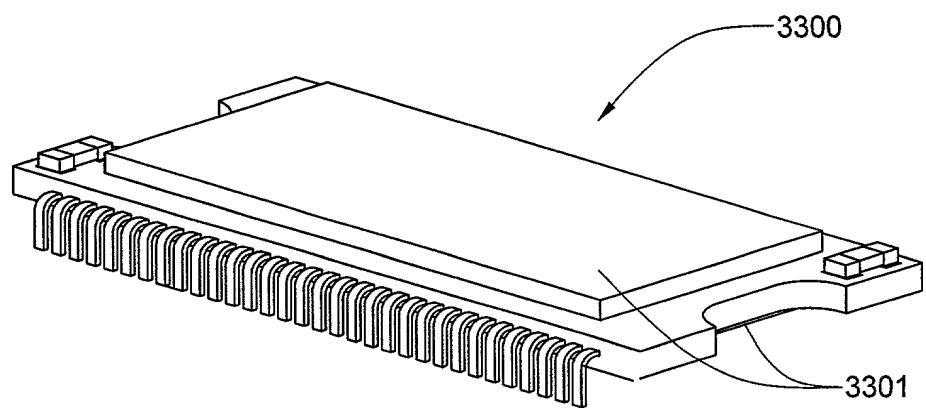
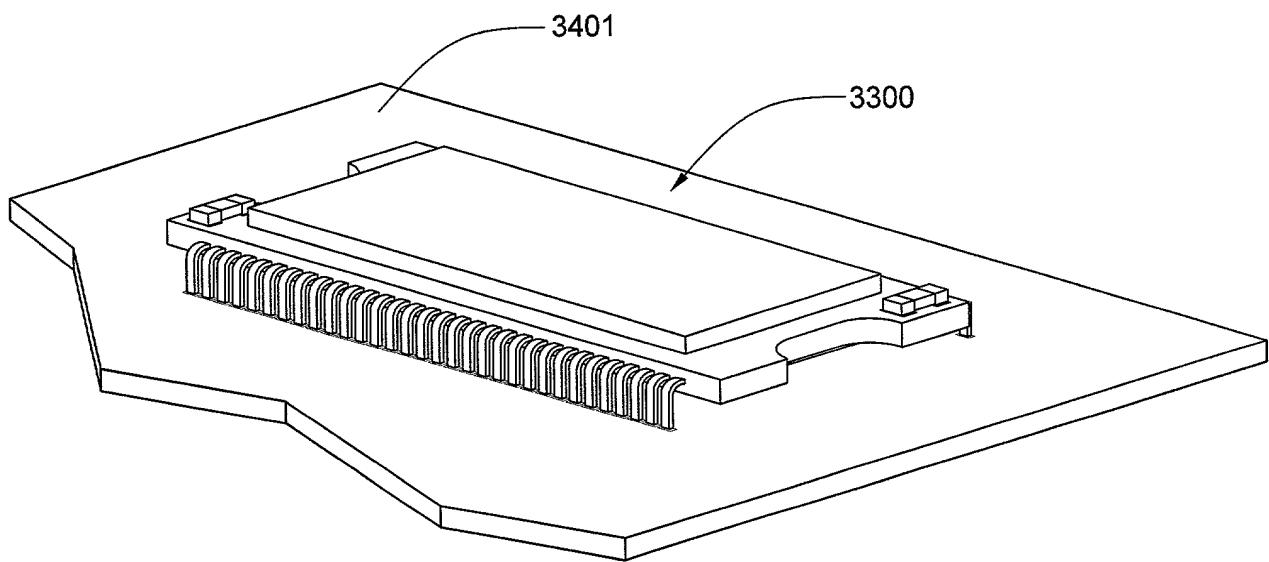


FIG. 32

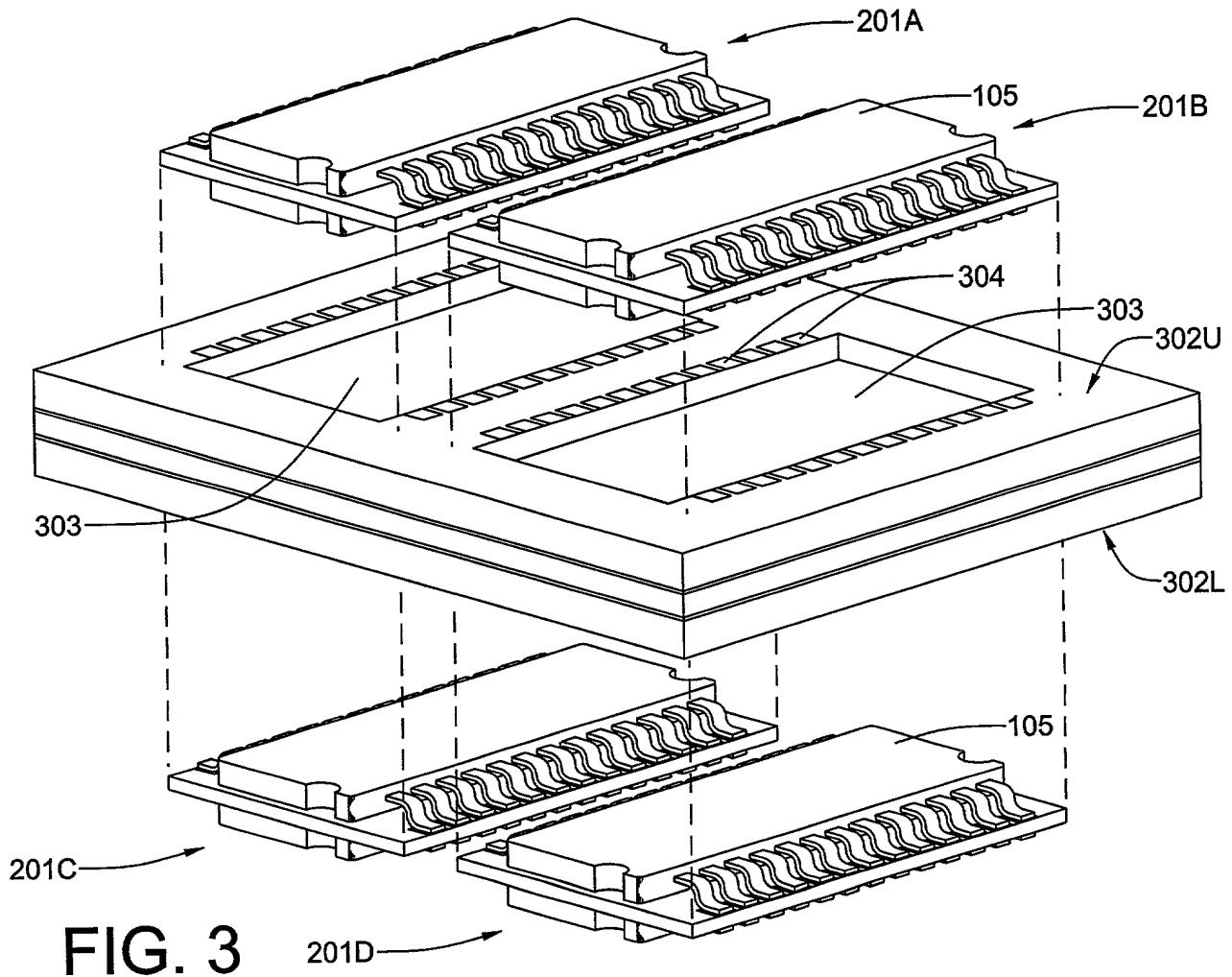
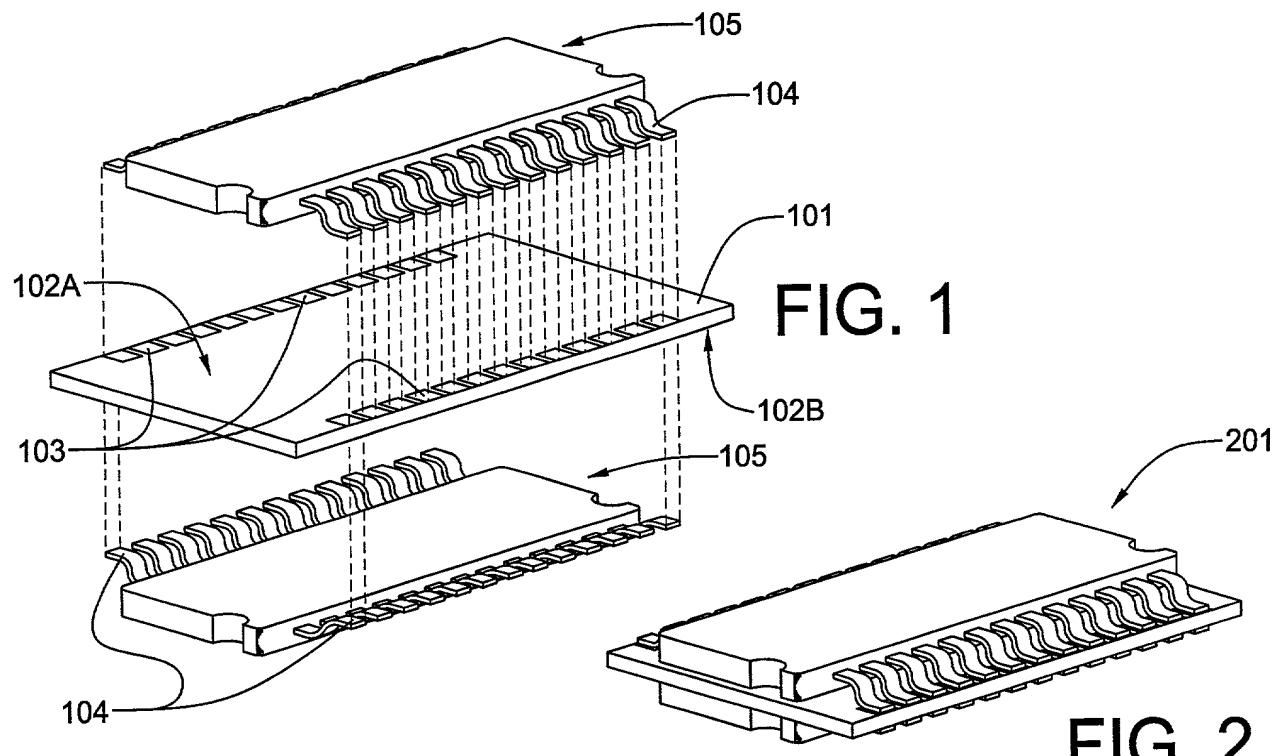


**FIG. 33**

005633000 "1976000



**FIG. 34**



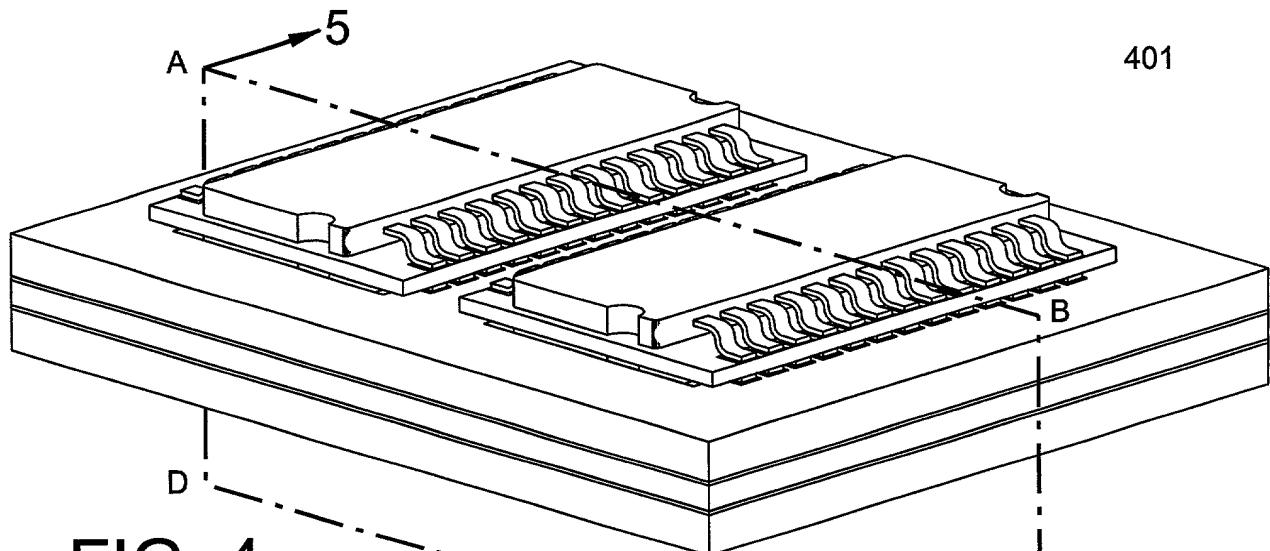


FIG. 4

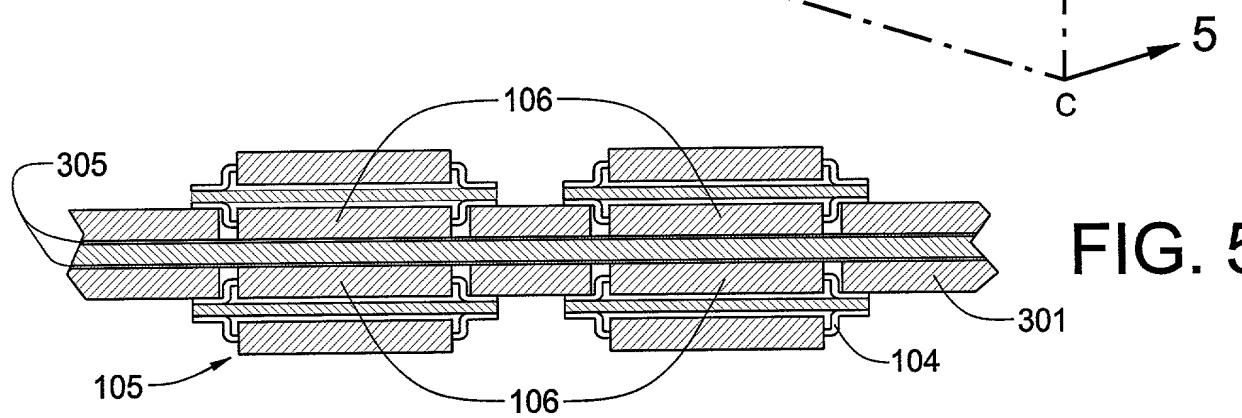


FIG. 5

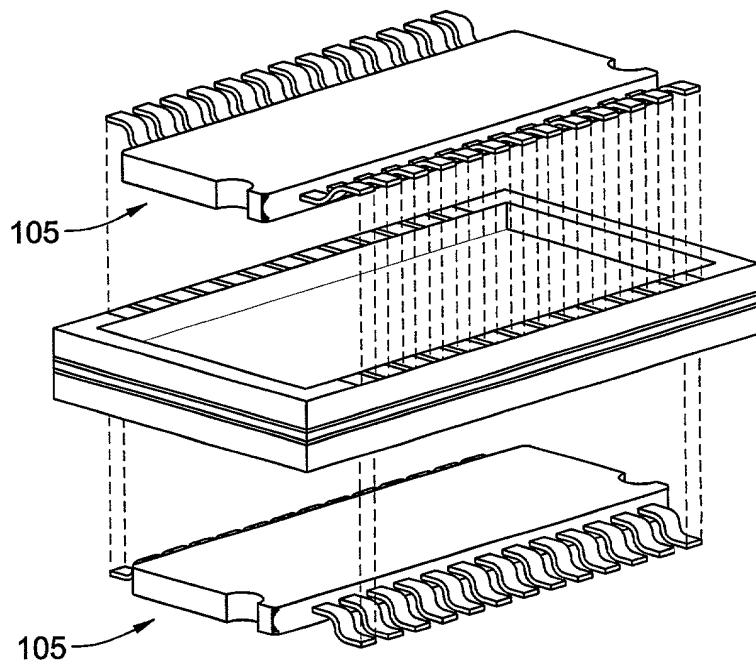
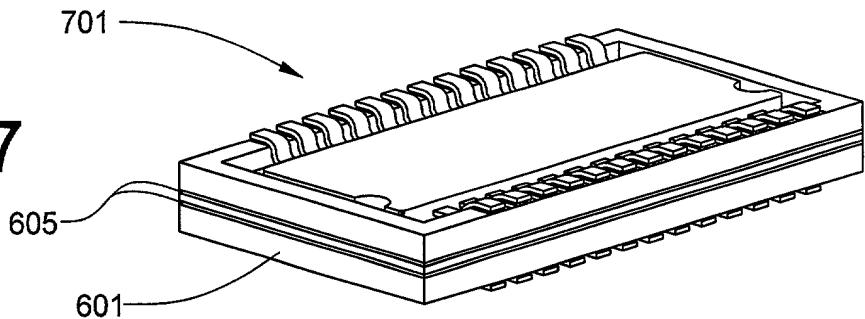


FIG. 6



**FIG. 7**

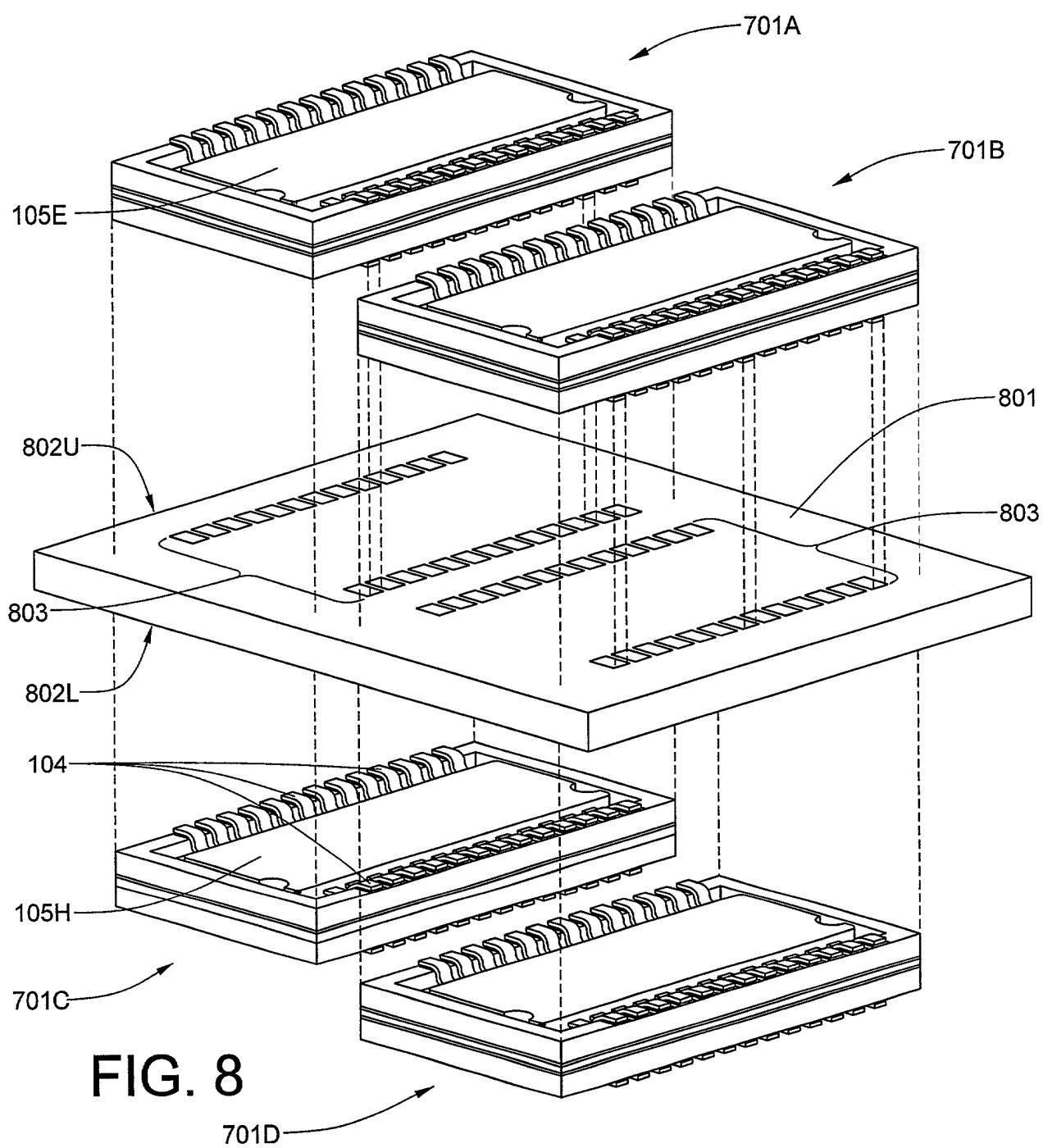


FIG. 8

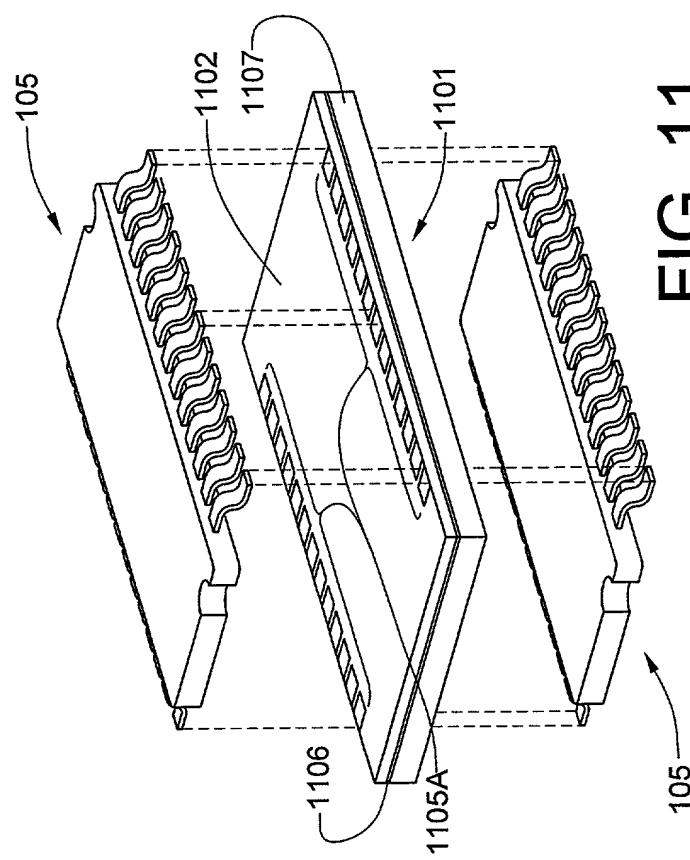


FIG. 11

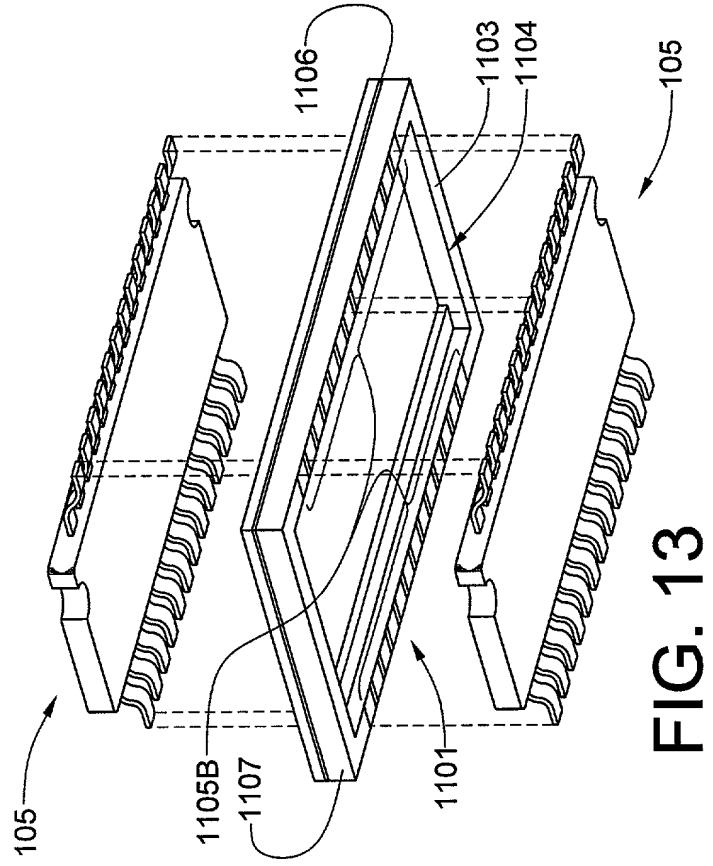


FIG. 13

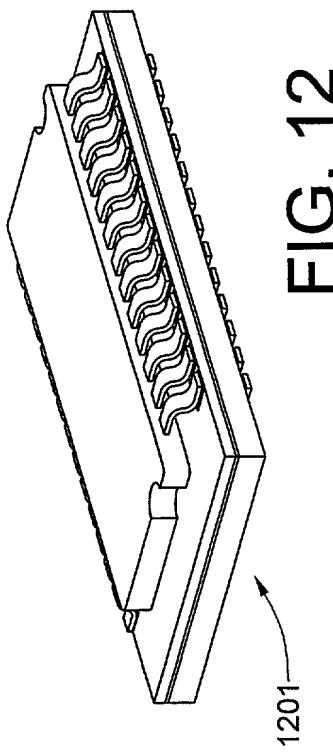


FIG. 12

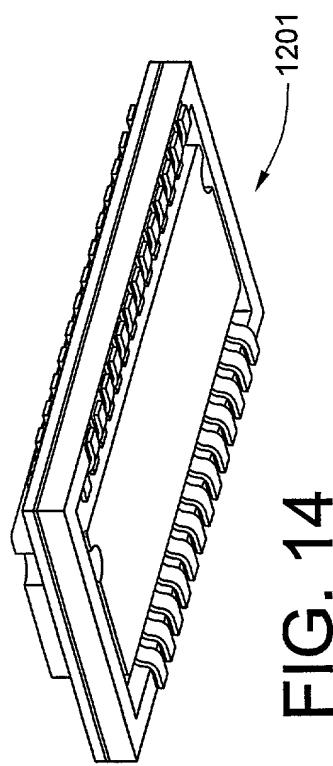
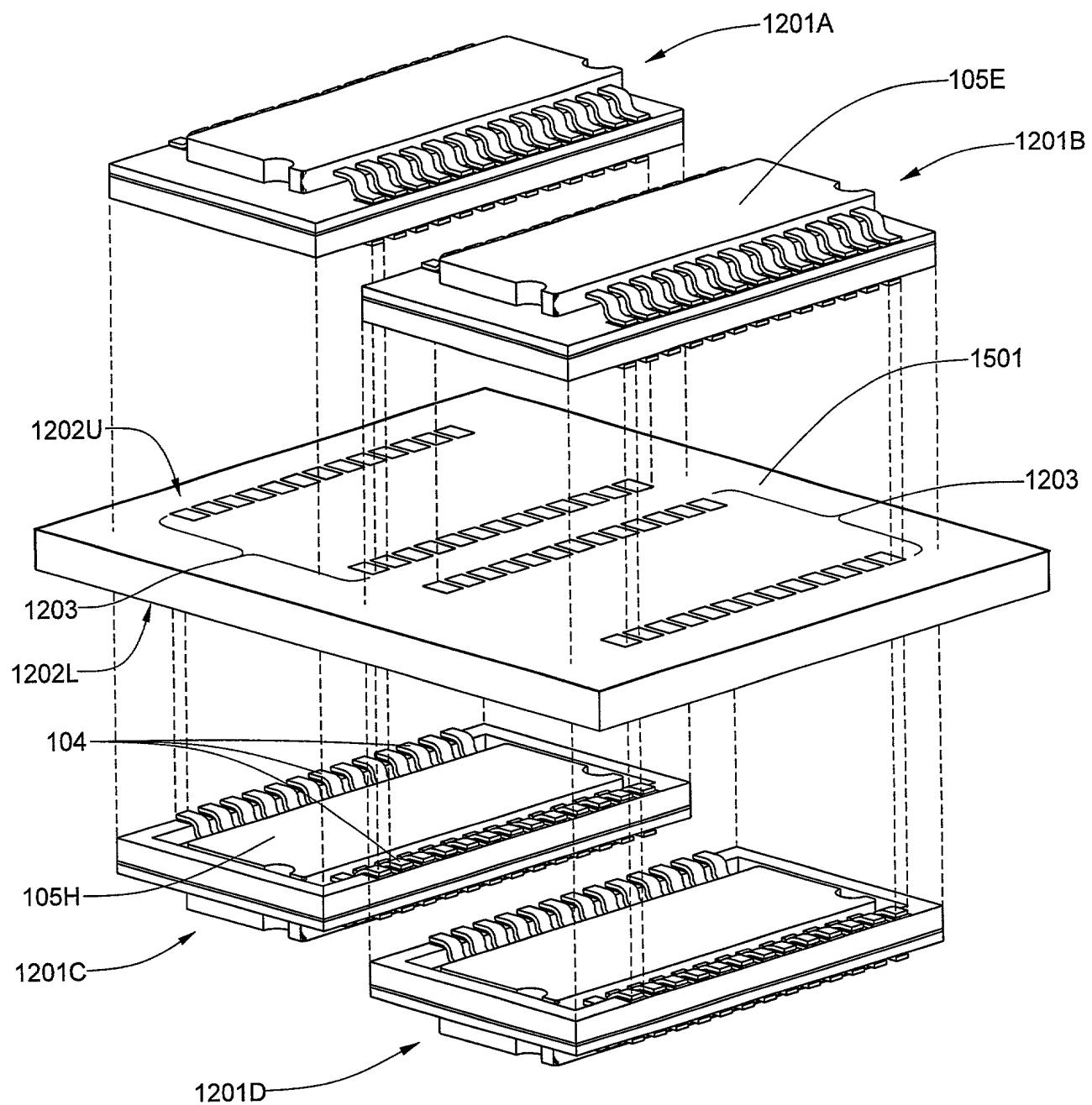


FIG. 14



**FIG. 15**

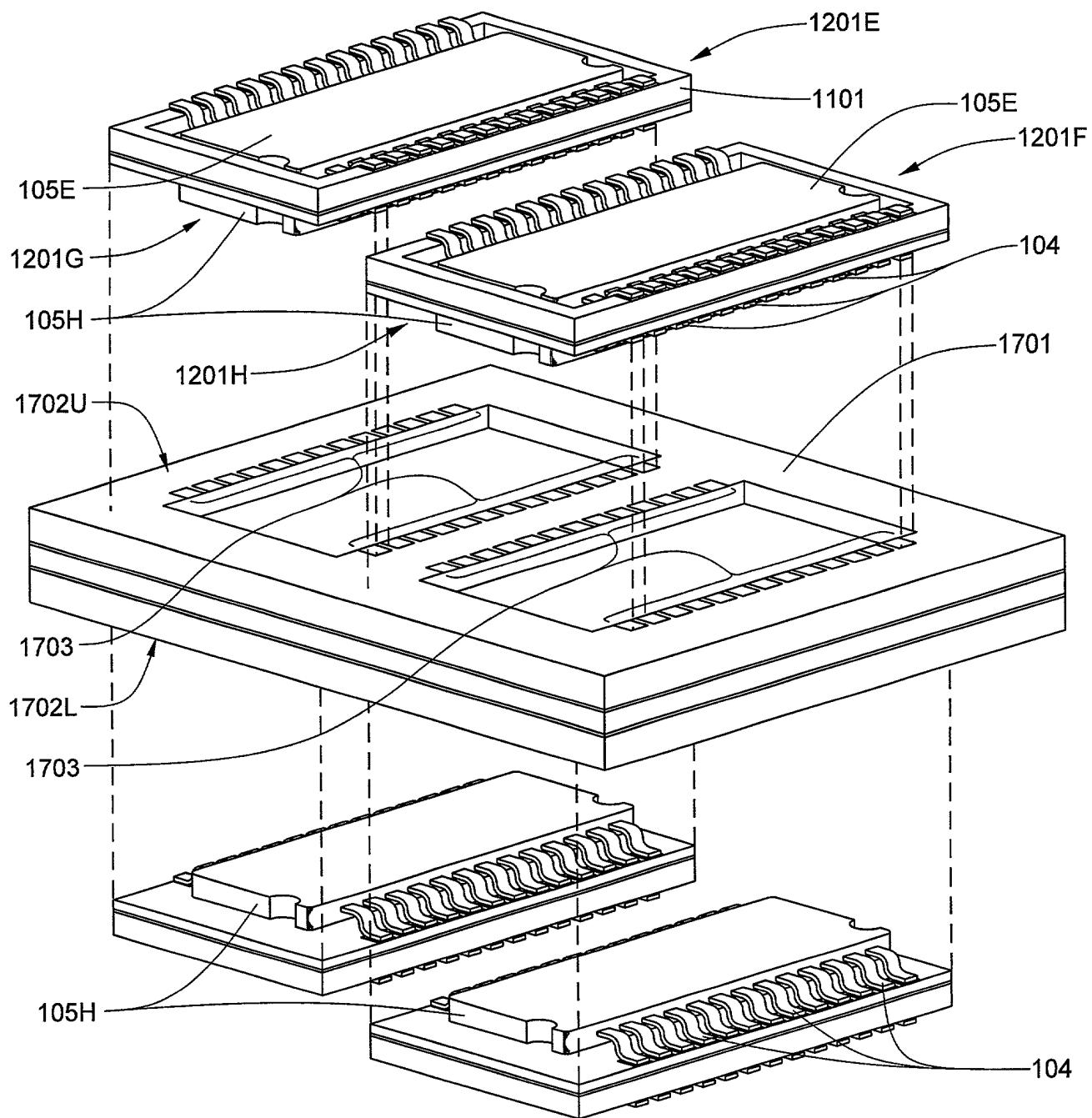
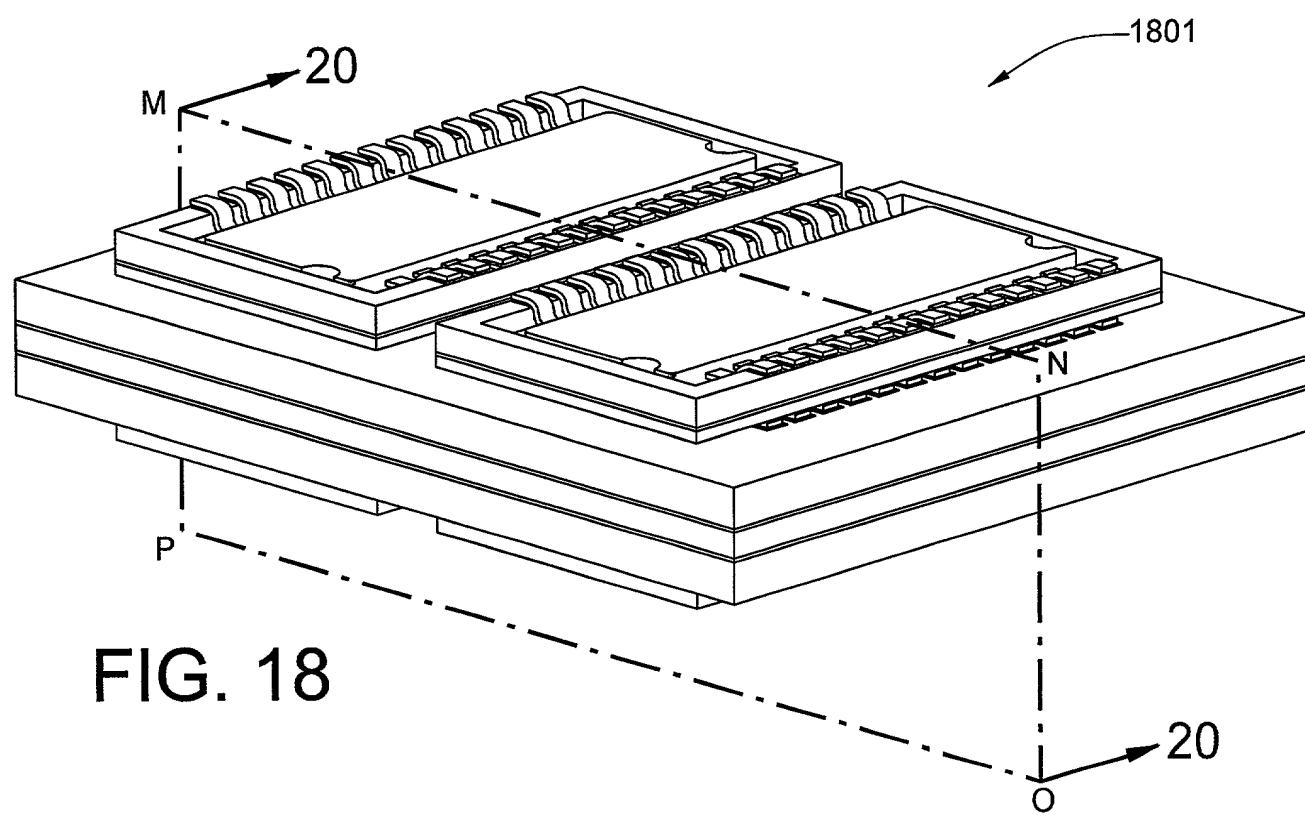
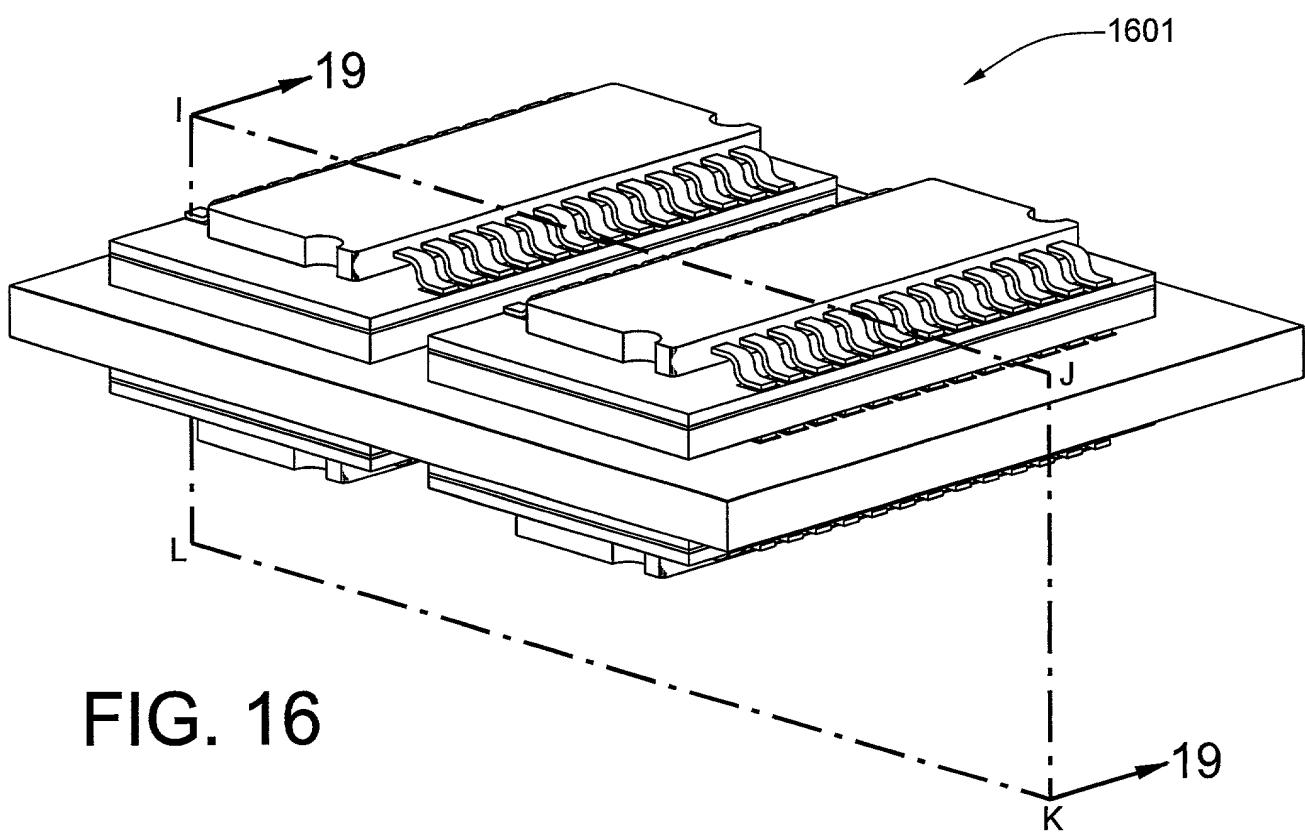


FIG. 17



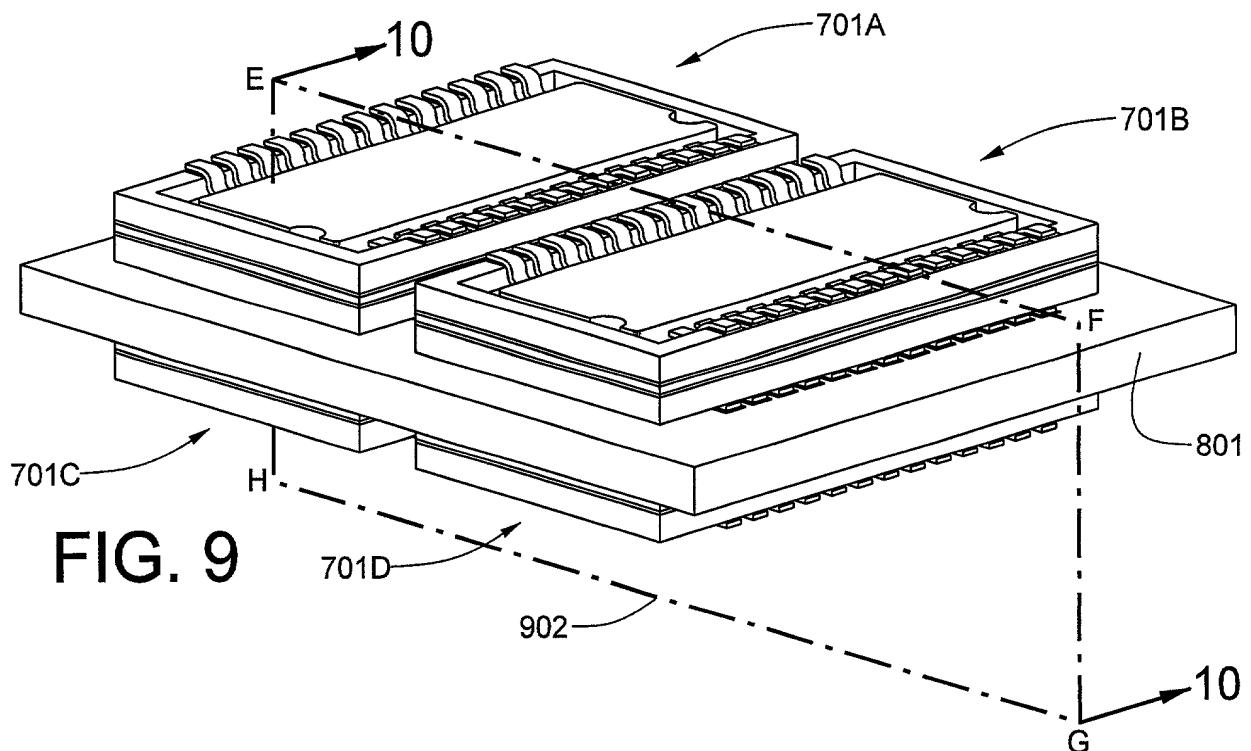


FIG. 10

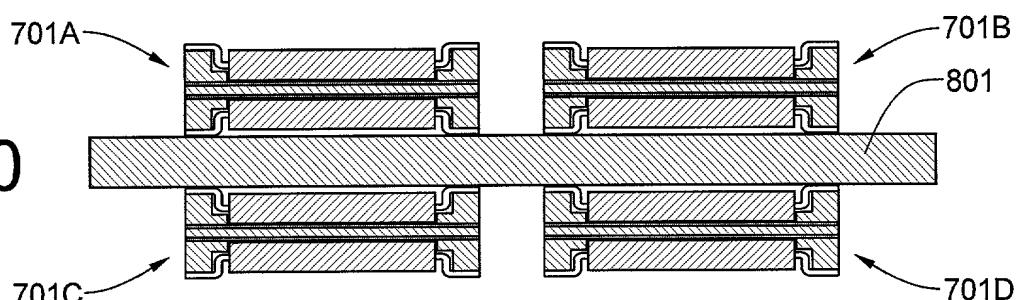


FIG. 19

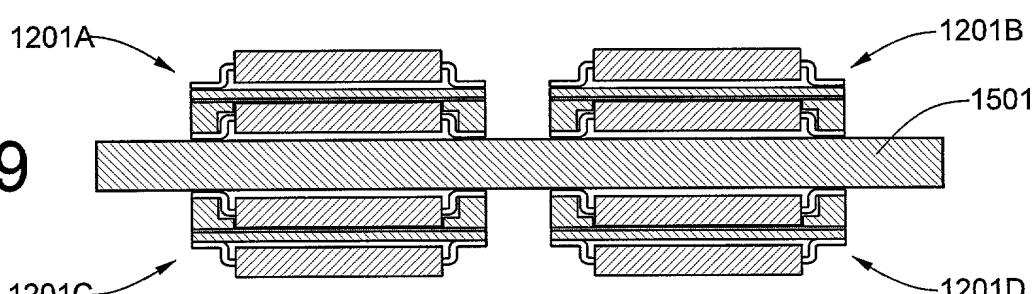
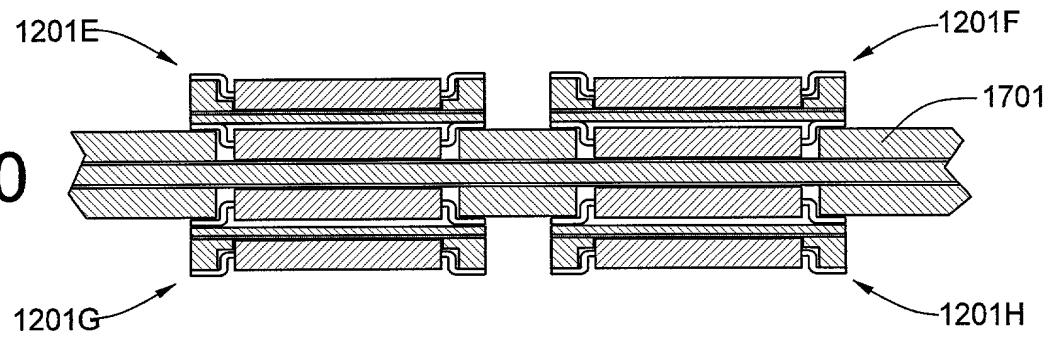
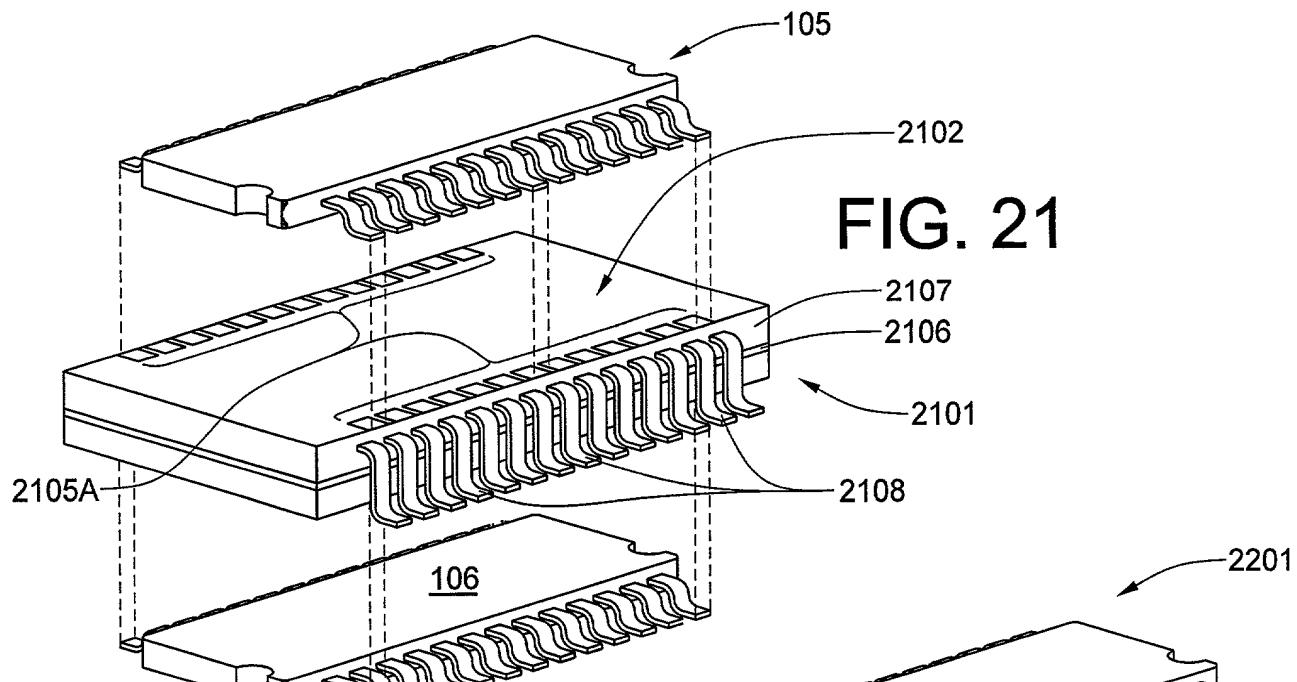
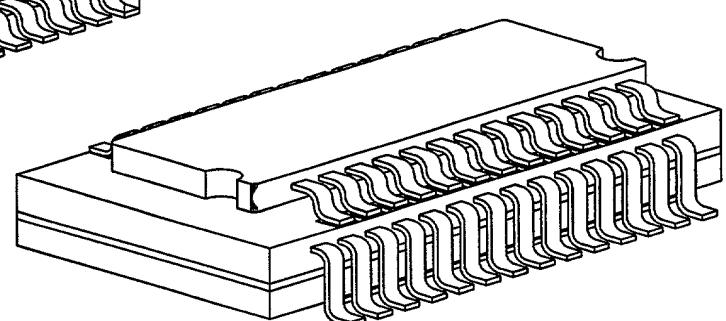


FIG. 20

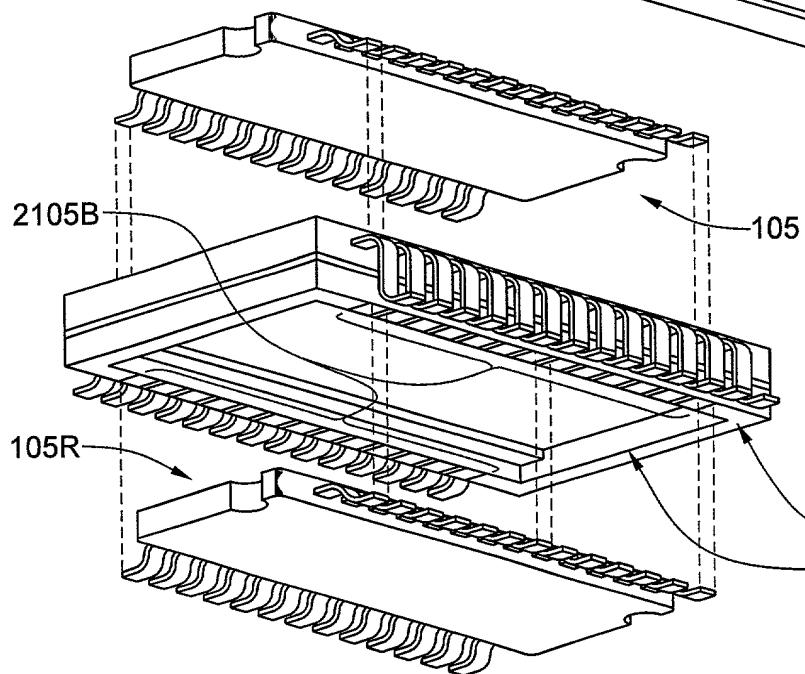




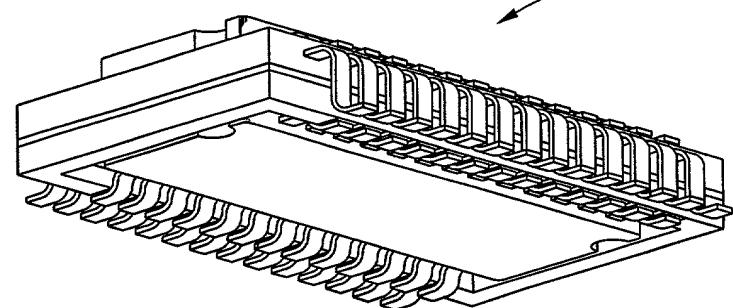
**FIG. 21**



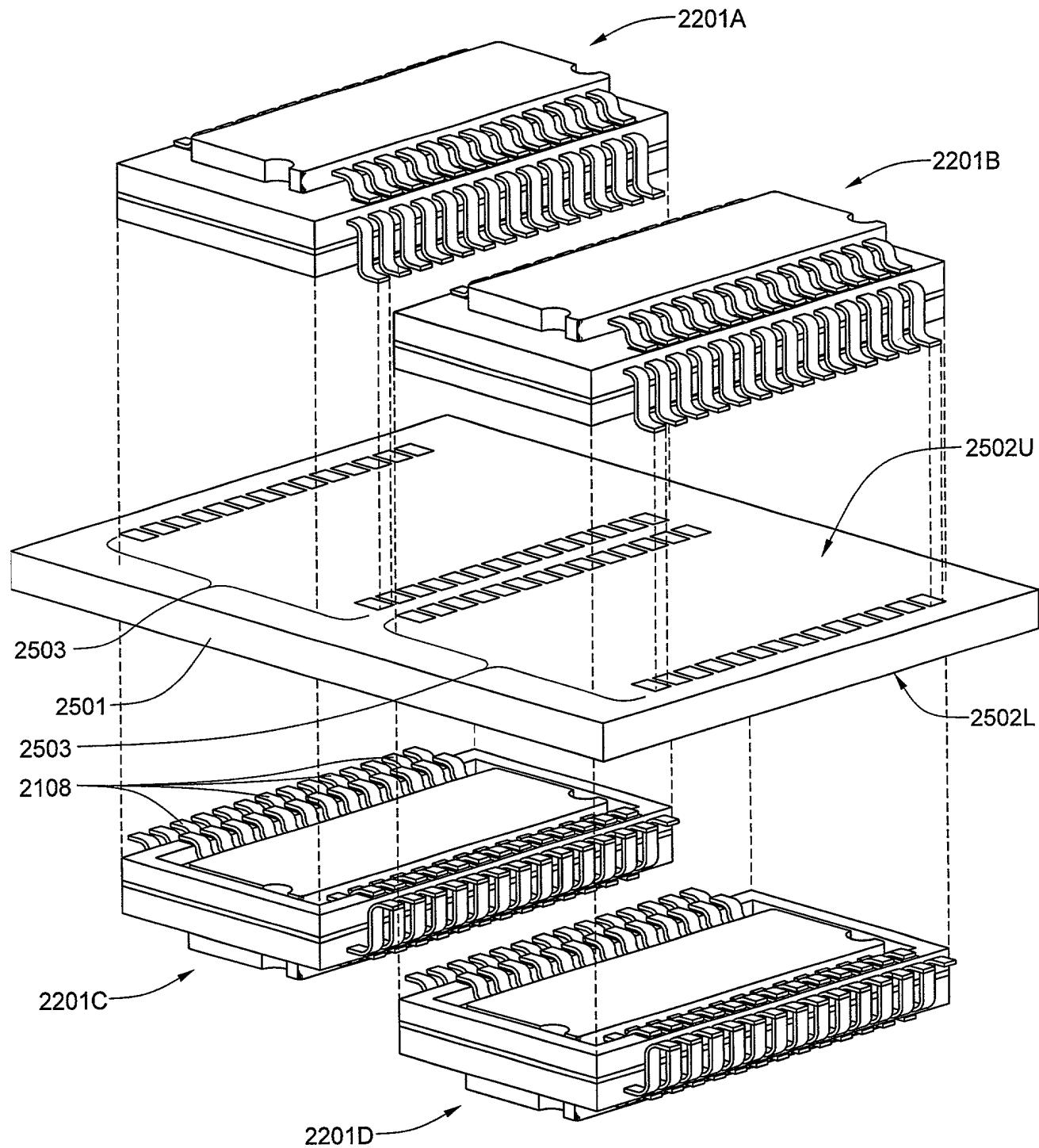
**FIG. 22**



**FIG. 23**



**FIG. 24**



**FIG. 25**

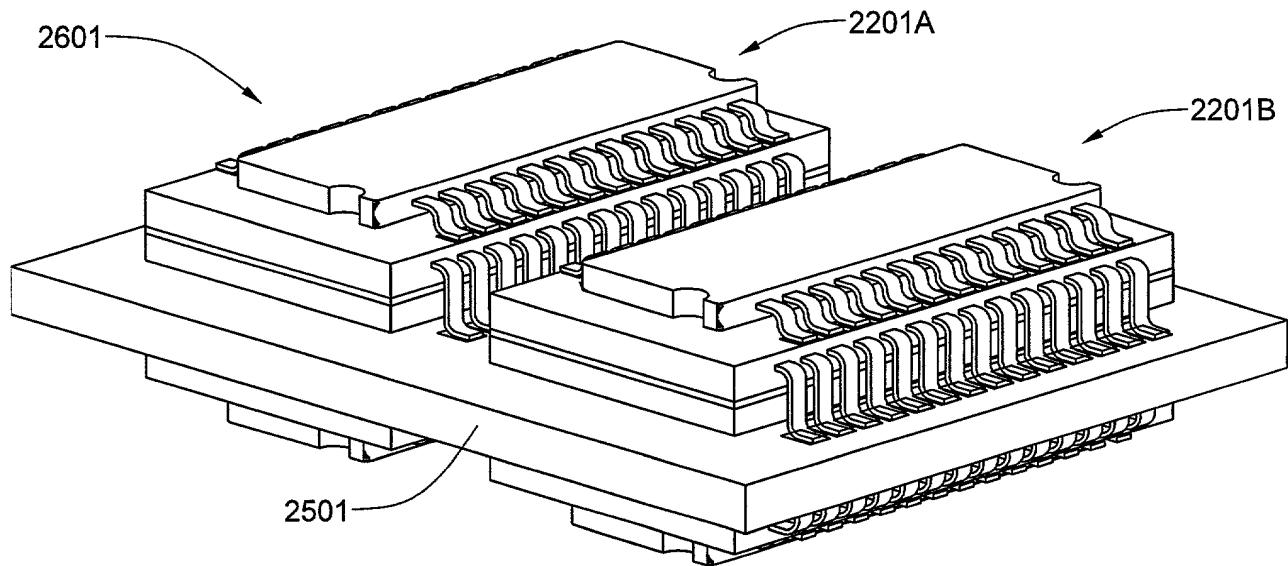


FIG. 26

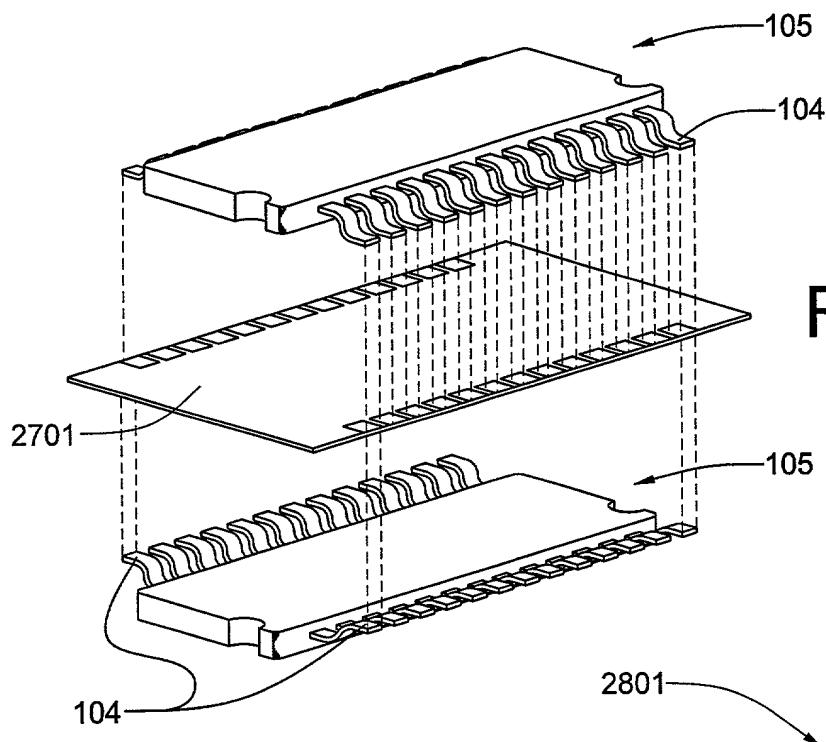


FIG. 27

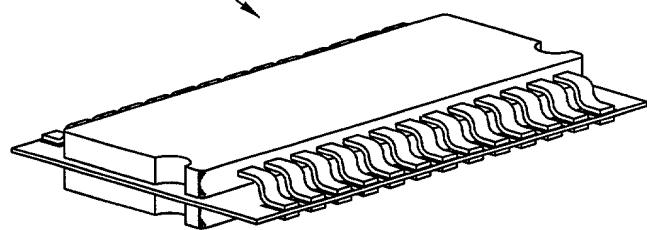
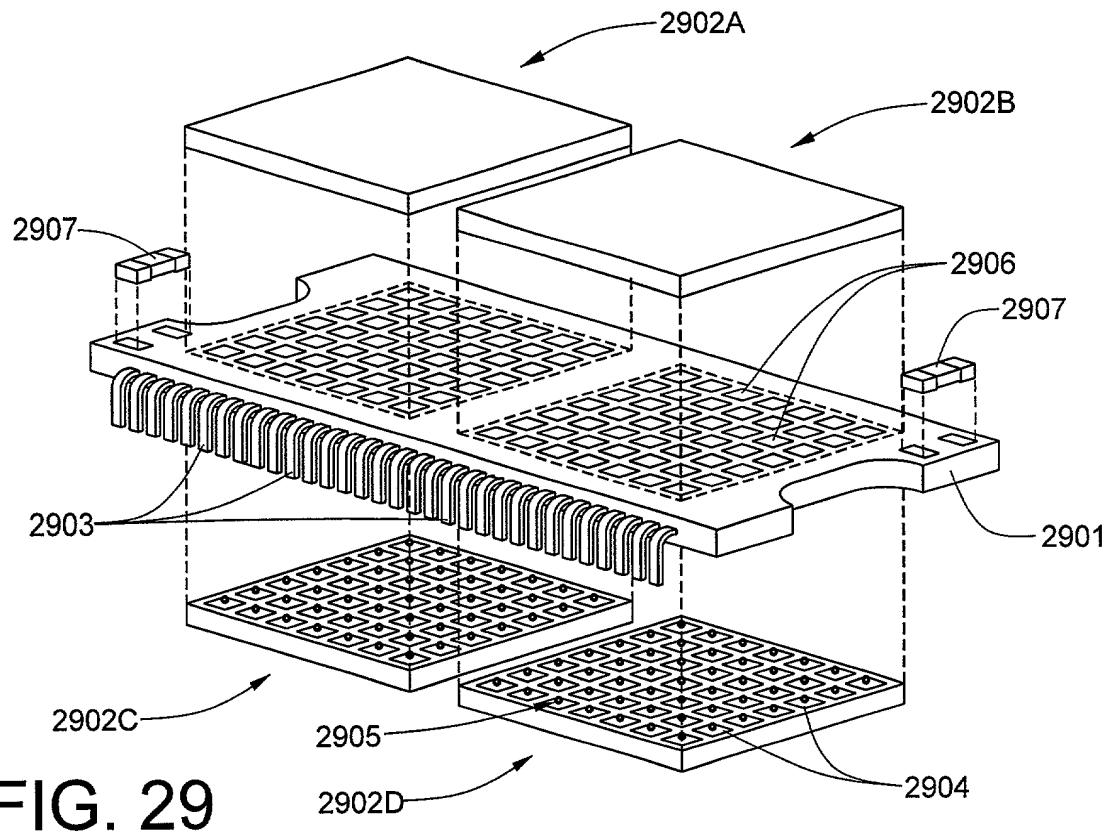
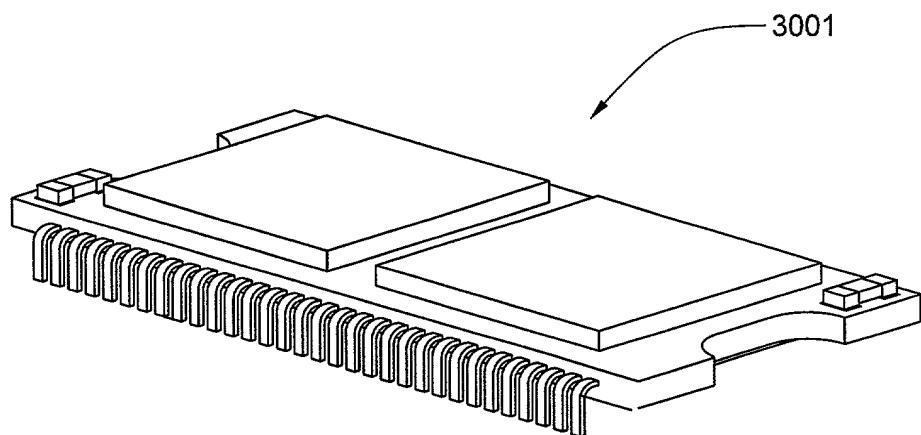


FIG. 28



**FIG. 29**



**FIG. 30**

00 9 7 0 7 0 0 9 8 9 5 0

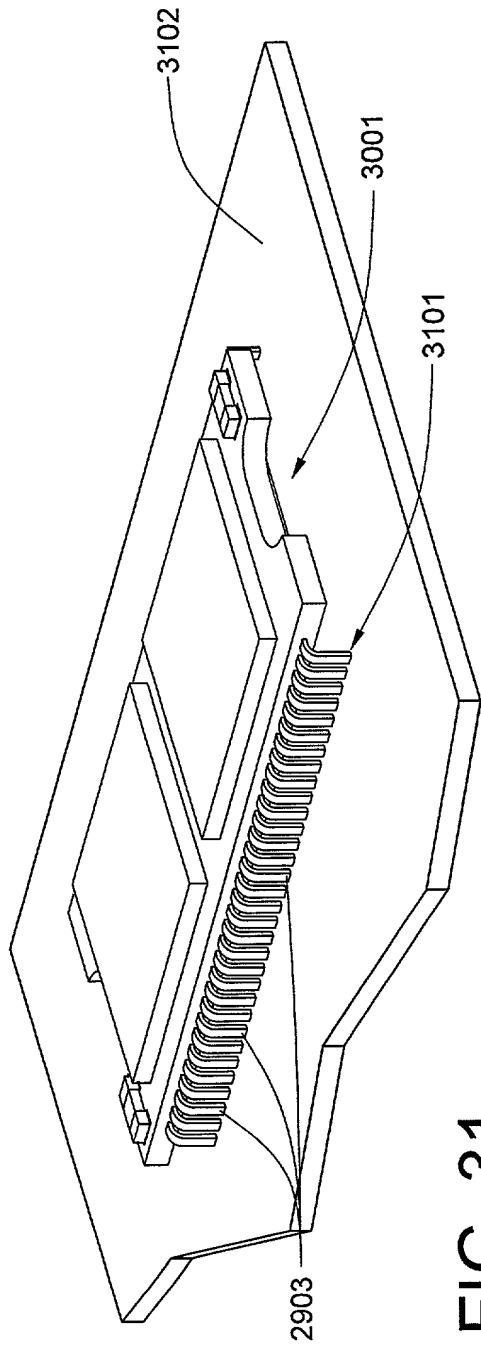


FIG. 31

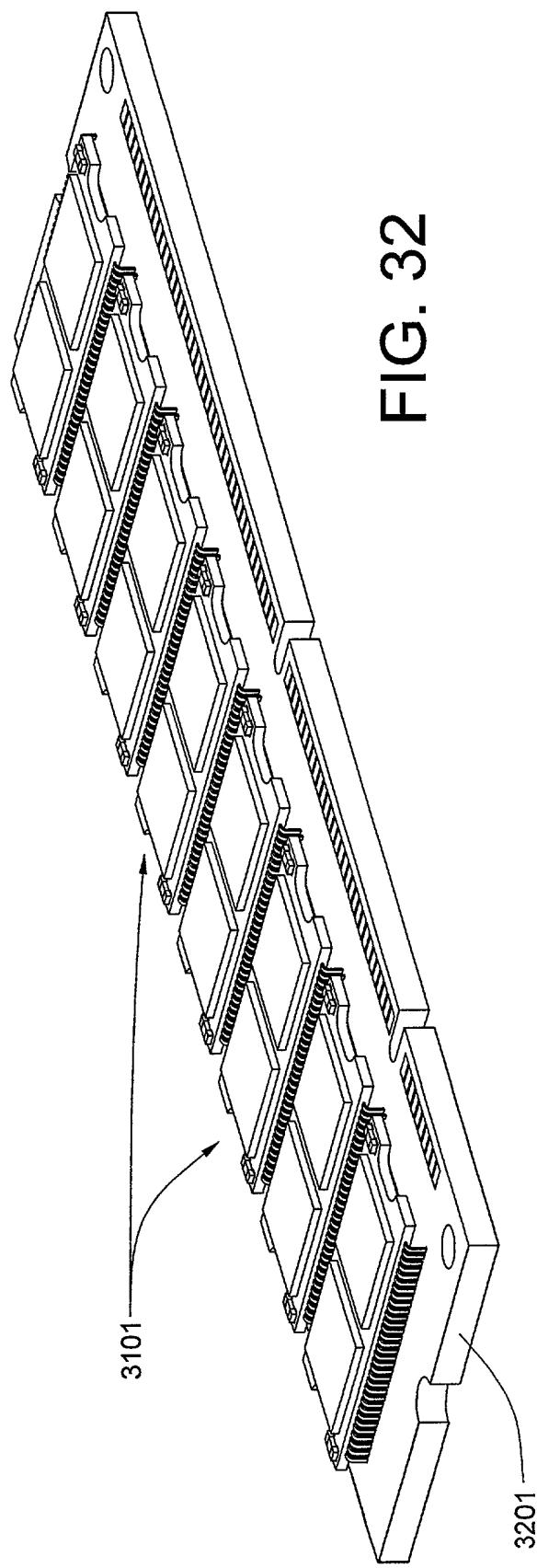
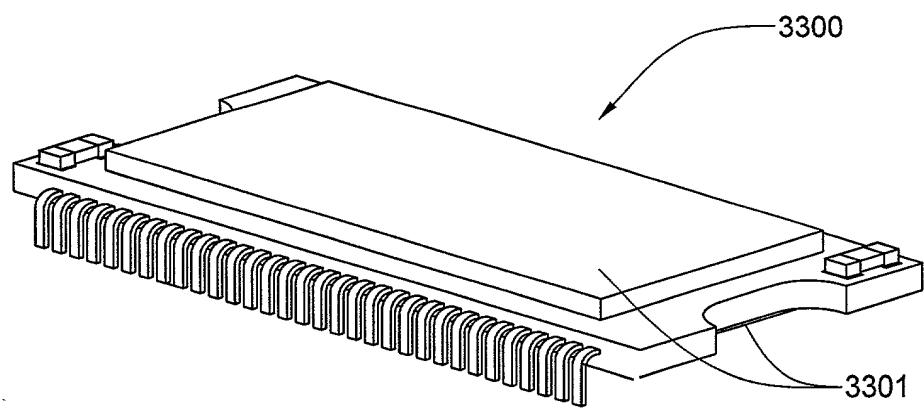
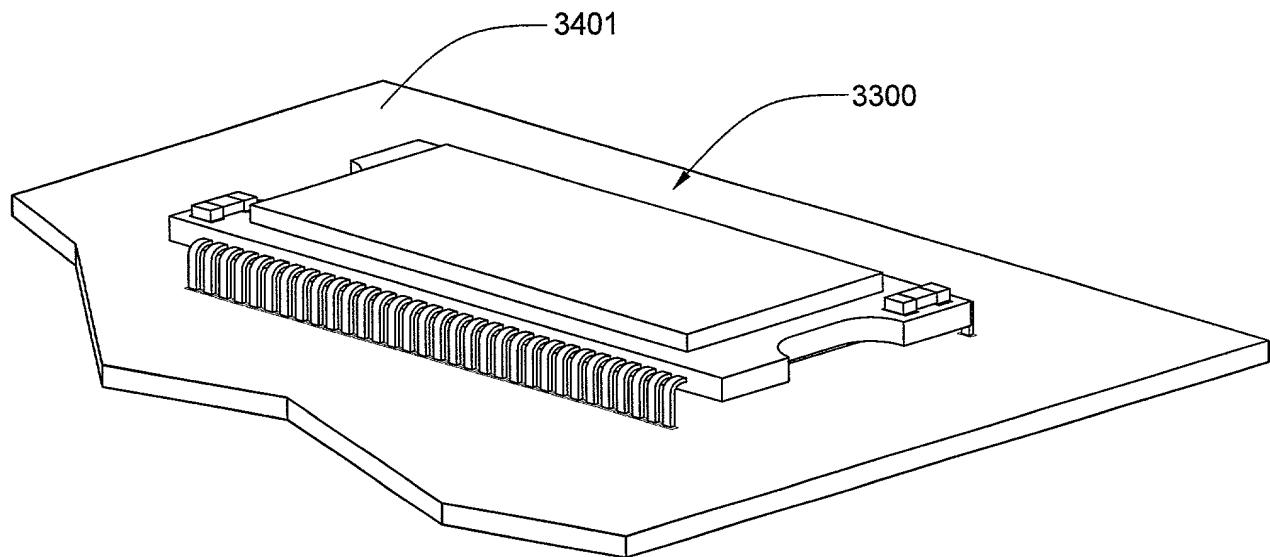


FIG. 32



**FIG. 33**

05000000000000000000000000000000



**FIG. 34**

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PTO/SB/01 (12-97)

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**DECLARATION FOR UTILITY OR  
DESIGN  
PATENT APPLICATION  
(37 CFR 1.63)**

Declaration Submitted with Initial Filing      OR       Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	LE99-02
First Named Inventor	Kenneth J. Kledzik
<b>COMPLETE IF KNOWN</b>	
Application Number	/
Filing Date	OCT 2000
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**CARRIER-BASED ELECTRONIC MODULE**

the specification of which

*(Title of the Invention)*

is attached hereto

OR

was filed on (MM/DD/YYYY)  as United States Application Number or PCT International

Application Number  and was amended on (MM/DD/YYYY)  (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?
			<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>

Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)	
		<input type="checkbox"/> Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

[Page 1 of 2]

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## DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:  Customer Number  →  Place Customer Number Bar Code Label here  
 OR  
 Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number
Angus C. Fox, III	31,828		

Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to:  Customer Number  OR  Correspondence address below

Name	Angus C. Fox, III				
Address	4093 N. Imperial Way				
Address					
City	Provo	State	UT	ZIP	84604-5386
Country	U.S.A.	Telephone	801-225-9000	Fax	801-224-7447

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor:	<input type="checkbox"/> A petition has been filed for this unsigned inventor
---------------------------------	-------------------------------------------------------------------------------

Given Name (first and middle if any)	Family Name or Surname
--------------------------------------	------------------------

Kenneth J.	Kledzik
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Inventor's Signature						Date	
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Residence: City	San Clemente	State	CA	Country	U.S.A.	Citizenship	U.S.A.
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Post Office Address	43 Via Sonrisa						
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Post Office Address							
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City	San Clemente	State	CA	ZIP	92673	Country	U.S.A.
------	--------------	-------	----	-----	-------	---------	--------

Additional inventors are being named on the \_\_\_\_\_ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

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<b>DECLARATION</b>		<b>ADDITIONAL INVENTOR(S)</b> <b>Supplemental Sheet</b> Page <u>1</u> of <u>1</u>
--------------------	--	-----------------------------------------------------------------------------------------

<b>Name of Additional Joint Inventor, if any:</b>		<input type="checkbox"/> A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])		Family Name or Surname					
Jason C.		Engle					
Inventor's Signature						Date	
Residence: City	San Clemente	State	CA	Country	U.S.A.	Citizenship	U.S.A.
Post Office Address	2400 South Ola Vista						
Post Office Address							
City	San Clemente	State	CA	ZIP	92672	Country	U.S.A.
<b>Name of Additional Joint Inventor, if any:</b>		<input type="checkbox"/> A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])		Family Name or Surname					
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Post Office Address							
Post Office Address							
City		State		ZIP		Country	
<b>Name of Additional Joint Inventor, if any:</b>		<input type="checkbox"/> A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])		Family Name or Surname					
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Post Office Address							
Post Office Address							
City		State		ZIP		Country	

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**STATEMENT UNDER 37 CFR 3.73(b)**Applicant/Patent Owner: Legacy Electronics, Inc.Application No./Patent No.: \_\_\_\_\_ Filed/Issue Date: 13 OCT 2000Entitled: CARRIER-BASED ELECTRONIC MODULELegacy Electronics, Inc., a California corporation,  
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1.  the assignee of the entire right, title, and interest; or
2.  an assignee of an undivided part interest

in the patent application/patent identified above by virtue of either:

A.  An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the Patent and Trademark Office at Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.

OR

B.  A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below.

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The document was recorded in the Patent and Trademark Office at  
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 Additional documents in the chain of title are listed on a supplemental sheet. Copies of assignments or other documents in the chain of title are attached.

NOTE: A separate copy (i.e., the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the PTO. See MPEP 302-302.8

The undersigned (whose title is supplied below) is empowered to sign this statement on behalf of the assignee.

10-16 2000

Date

Signature

Jason C. Engle

Typed or printed name

Title